Synopsys, IBM, Chartered and ARM Collaborate to Extend Low-Power 90nm Reference Flow

Flow Supports IC Compiler for Common Platform's Low-Power Process

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that it has delivered an enhanced version of its RTL-to-GDSII low-power reference design flow for the latest 90-nanometer (nm) process offered as part of the IBM-Chartered Semiconductor Manufacturing Common Platform. Combining the latest shared 90-nm low-power process technology from the Common Platform, the ARM® Metro™ low-power products, part of its family of Artisan® physical IP, and Synopsys' expertise in design flows with a full complement of Synopsys Galaxy™ Design Platform implementation products, including IC Compiler, the reference design flow enables rapid design of highly complex devices while addressing signal integrity and power reduction requirements.

The reference flow allows designers to easily and accurately maintain process technology files, ARM Metro memories and standard cell and I/O libraries, and design data in a single consistent directory structure. This flow uses advanced methodologies that take the designer through each step of the design process, maintaining data consistency through the Milkyway™ database and shared design constraint files. The reference flow is consistent with the design flow in Synopsys Pilot Design Environment and can be extended and enhanced by designers to address design-specific requirements. Chartered and IBM have validated the complete reference flow on the Common Platform 90-nm process using ARM Metro physical IP.

The reference flow supports both flat and hierarchical design techniques and includes Synopsys' IC Compiler, a next-generation place-and-route system. IC Compiler transcends current generation solutions by offering three new technologies: Extended Physical Synthesis (XPS), Signoff Driven Design Closure, and Design for Yield. These differentiating technologies allow IC Compiler to provide superior results and faster time-to-results. Manufacturability is also addressed in the place-and-route technology files. IC Compiler has a unified, TCL-based architecture that includes physical synthesis, placement, routing, yield, signal integrity (SI), test, and low-power design. The resulting design can be manufactured at IBM or Chartered using the same GDSII file.

"The latest version of the Synopsys low-power reference flow provides important technology like IC Compiler and capabilities such as hierarchical physical design, allowing designers to create complex chips that minimize power and maximize performance," stated Steve Longoria, vice president, Semiconductor Technology Platform for IBM Systems and Technology Group. "Coupling the complete Synopsys design flow with the Common Platform's low-power 90-nanometer process technology gives chip designers both next-generation design capability and manufacturing flexibility for their projects."

"Chartered and IBM have worked closely with Synopsys to refine and validate this reference flow using our latest technology files and we have independently validated the flow by taking a design all the way from RTL to verified GDSII," said Kevin Meyer, vice-president of worldwide Marketing and Platform Alliances at Chartered. "Our validation of this reference flow demonstrates that customers will be able to apply it to their designs to create chips ready for manufacturing at Chartered or IBM with no re-work required."

"ARM is excited to be continuing to drive the industry agenda for low power in a broad range of consumer devices," said Neal Carney, vice-president of Marketing, Physical IP, ARM. "The collaboration between ARM, IBM, Chartered and Synopsys provides real benefits to designers in delivering a low risk, proven path from design to silicon. The combination of proven physical IP, process technologies, and a complete design methodology is a major step forward for creation of the next-generation of 90-nanometer low-power devices."

"The close collaboration between IBM, Chartered, ARM, and Synopsys has resulted in significant benefits for our customers such as reduction in project risk and time-to-production," said Guri Stark, vice president of Marketing, Solutions Group at Synopsys. "We have combined the latest Synopsys tools, the design and design flow expertise of our Professional Services team, the latest 90-nanometer low-power technologies from IBM and Chartered, and the new ARM Metro libraries to produce a complete solution for next-generation designs."

Availability

The reference flow is available today at no charge to Synopsys customers and may be obtained via Synopsys' SolvNet online support site at www.solvnet.synopsys.com.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com.

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