Synopsys Advances Testbench Performance and Productivity With Vera 6.2

Enhanced Constraint Solver Delivers up to 10x Faster Performance; Vera Combines Support for Object- and Aspect-oriented Programming

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Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced the latest release of its Vera® advanced testbench automation tool, an integral part of the Synopsys Discovery™ Verification Platform. Key enhancements to Vera include an enhanced constraint solver, support for aspect-oriented extensions to object-oriented programming, and additional productivity features. Vera 6.2 delivers up to 10x faster constraint-solver performance, enabling verification engineers to generate a large number of high-quality tests, in a shorter period of time. Vera 6.2 also offers enhanced testbench development productivity and flexibility by extending its object-oriented programming model with aspect-oriented capabilities. This powerful combination of programming styles enables engineers to create verification environments that are both easier to develop and efficient to maintain.

"StarGen's serial switched interconnect chipsets require a testbench solution with a powerful constraint solver to enable us to achieve our quality and time-to-market goals," said Lynne Brocco, vice president of Hardware Engineering at StarGen, Inc. "Vera's fast constraint solver with its ability to solve constraints over arrays is ideally suited for our Advanced Switching industry standard designs. The tool has enhanced productivity and simulation throughput, which is essential when verifying the rich functionality of our latest products."

Vera 6.2 features enhanced constraint-solving engines that are up to 10x faster, enabling it to generate more high-quality tests in less time. A significant enhancement to the solver engine is the capability to simultaneously solve constraints over arrays, allowing engineers to more quickly and easily generate complex sequences of transactions. This capability can be used to generate multiple streams of network traffic and to verify deeply pipelined processors and digital signal processor designs. Vera's flexible constraint solver helps engineers exhaustively verify corner cases and tape-out their designs with higher confidence.

Testbench Development Productivity Enhancements

Vera 6.2 enhances its object-oriented programming model with aspect-oriented extensions to provide increased testbench-coding productivity. Object-oriented programming is essential to create a well-structured testbench foundation that is easy to maintain. The addition of aspect-oriented extensions helps engineers to quickly and easily create individual tests built on this testbench foundation, thus improving test-writing productivity.

"Vera's support of object-oriented programming with aspect-oriented extensions should allow us to refine our testbenches faster and with less effort," said Jason Sprott, engineering director at Verilab, Ltd. "The addition of aspect-oriented extensions to Vera further enhances its capability and improves the productivity of engineers dealing with the challenges of verification code development today."

Additional productivity enhancements in Vera include SmartQ, an intelligent queue construct. SmartQ supports multiple data types and provides a rich set of methods to analyze and manipulate queue elements. The use of SmartQ enables engineers to efficiently create powerful self-checking tests.

"Cray develops extremely large, complex designs and uses Vera to help meet aggressive schedules while achieving high-verification quality," said Greg Faanes, senior engineering manager, Design, at Cray Inc. "Vera has enabled a two- to three-fold increase in real-world verification productivity at Cray, allowing us to complete our verification environment before the RTL is available. Vera has been easy for our team to learn, with new users becoming productive in under a week."

"Customers choose to use Synopsys' Discovery Verification Platform because of its best-in-class technologies and industry-leading integration," said Swami Venkat, director of marketing, RTL Verification, Synopsys Verification Group. "With Vera 6.2, we have further raised the bar on testbench automation with faster performance and advanced productivity, and will continue to enhance Vera to enable our customers to meet their ever-increasing verification challenges."

Availability

Vera 6.2 is available now. For more information on Vera, please visit https://www.synopsys.com/verification/static-and-formal-verification.html .

Synopsys Discovery Verification Platform

The Discovery Verification Platform is a unified environment that provides high performance and efficiency of interaction among all platform components, including mixed-HDL simulation, mixed-signal, system-level verification, assertions, verification intellectual property, code coverage, functional coverage, testbenches and formal analysis. Combined with SystemVerilog and Synopsys' design-for-verification methodology, the Discovery Verification Platform helps designers achieve higher levels of verification productivity by contributing to first-time silicon success within required project cycles.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading IC design and verification platforms to the global electronics market, enabling the development of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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