Synopsys Announces EDA Industry's First Verification IP Library for SystemVerilog With Methodology Support

VCS Verification Library Enables Rapid Adoption of SystemVerilog With Full Support of the Verification Methodology Manual (VMM) for SystemVerilog

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that its VCS® Verification Library, containing DesignWare® verification intellectual property (VIP), is first to support testbenches created using IEEE Std 1800™-2005 SystemVerilog and the coverage-driven methodology defined in the Verification Methodology Manual (VMM) for SystemVerilog, published by Springer Science+Business Media. Verification engineers who use SystemVerilog for testbench development now have access to a proven portfolio of Synopsys VIP to decrease the cost of testbench development, speed the time to reach coverage goals, and reduce risk in order to meet project schedules. Verification IP support for SystemVerilog provides engineers with crucial building blocks for the development of more effective testbenches to address the challenge of system-on-chip (SoC) verification. This support enables more than 600 companies that use DesignWare verification IP to adopt a coverage-based verification methodology based on SystemVerilog and the VMM for SystemVerilog.

As the standard interfaces on SoC designs continue to increase in number and complexity, verification engineers are faced with tremendous challenges. Synopsys is leading the effort to solve these challenges with verification IP that helps simplify the creation of VMM-compliant testbenches and provides protocol-specific coverage. When combined with Native Testbench in the VCS solution, DesignWare Verification IP delivers up to 5X improvement in verification performance.

"With a considerable increase in the verification challenge for SoCs, verification engineers are asking for proven and fully-featured verification IP to reduce testbench development time and radically improve their verification productivity," said Guri Stark, vice president of Marketing, Solutions Group, Synopsys, Inc. "Providing a broad portfolio of verification IP with SystemVerilog support, including support for the VMM for SystemVerilog, will accelerate customer adoption of a new generation of more effective verification techniques that will increase verification coverage and significantly reduce project schedule risk."

The VMM for SystemVerilog provides verification engineers with a robust, consistent methodology for developing testbenches that help engineers meet the challenges of verifying today's complex SoC designs. The book defines a reusable constrained-random environment based on a coverage-driven methodology to increase verification productivity and quality. The verification IP contained in the VCS Verification Library provides essential SoC verification building blocks for VMM-compliant environments, resulting in a significant improvement for verification productivity.

"Synopsys' broad portfolio of standards-based verification IP with support of the Verification Methodology Manual for SystemVerilog signals the growing momentum for SystemVerilog," said Janick Bergeron, moderator of Verification Guild, co-author of the VMM for SystemVerilog and scientist at Synopsys, Inc. "The combination of Synopsys' high-quality verification IP and the VMM for SystemVerilog is a major step toward addressing the need for a standard methodology to verify complex SoCs based on an open, industry-standard language."

Pricing and Availability

Current customers of DesignWare Verification IP can gain access to the new functionality at no additional charge by requesting the SystemVerilog version from the Synopsys website. DesignWare Verification IP is available in the DesignWare Library, in the VCS Verification Library and as individual suites.

About VCS Verification Library

The VCS Verification Library, containing DesignWare Intellectual Property (VIP), provides a broad portfolio of design-proven, standards-based VIP helping designers save testbench development time and reach functional coverage goals faster. It offers advanced functionality for block and chip-level verification and is an integral part of the Synopsys Discovery™ Platform. VCS Verification Library supports Verilog, SystemVerilog, OpenVera® and VHDL testbenches. It supports all popular simulators and enables up to five times faster verification when used with the VCS solution. The VCS Verification Library includes verification IP for the following: PCI Express®, USB 1.1/2.0/OTG, AMBA™ 2.0 AHB™/APB, AMBA 3 AXI™, 10/100/1G/10G Ethernet, PCI 2.3, PCI-X® 1.0/2.0, I2C, SATA, Serial I/O standard protocols as well as more than 10,000 memory models and more. For more information on the VCS Verification Library, visit:

www.synopsys.com/products/solutions/discovery_platform.html.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits of using Synopsys' verification IP with SystemVerilog support. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties in the use of Synopsys' verification IP on customer designs, uncertainties attendant to any new design or verification methodology and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended January 31, 2006 entitled "Management's Discussion and Analysis of Financial Condition and Results of Operations -- Factors That May Affect Future Results."

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