Synopsys Introduces Next Generation 1-Pass Test Synthesis Enabling Deep Submicron Test For Mainstream Designs

DFT Compiler Max Delivers 10-50x Test Time Reduction in the Smallest Area With the Ease of 1-Pass Scan Synthesis

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced DFT Compiler MAX, its next generation DFT synthesis solution, offering 1-pass test data volume compression capabilities to address design and test challenges occurring in 130-nm and smaller process technologies. DFT Compiler MAX is an extension of Synopsys' unique 1-pass test synthesis solution that delivers push-button test data volume compression of 10-50x, enabling deep submicron (DSM) testing for high fault coverage without significant impact on test costs. The solution is transparently integrated within Synopsys' Design Compiler® and the entire Galaxy™ Design Platform to achieve best timing closure and to help eliminate costly iterations between design and test implementations by designers with minimal test expertise.

Deep-submicron (DSM) designs at 130-nm and below are becoming mainstream, bringing a new class of faults which cannot be detected with traditional stuck-at test techniques. These faults, such as resistive via and bridging faults, can only be detected with at-speed and bridging test, resulting in more test vectors leading to higher costs. Existing compression techniques being used to reduce test data volume require significant expertise and are difficult to integrate into the implementation flow. DFT Compiler MAX's unique Adaptive Scan technology removes the need for expertise, while delivering test compression with the smallest area. Concurrently, this new Adaptive Scan technology generates an efficient scan architecture which leads to minimum test application time. DFT Compiler MAX addresses design needs at 130-nm and below by enabling high quality test compression for both stuck-at and at-speed test, resulting in higher quality test without significant additional cost or design effort.

"Today's competitive market is driving us to reduce IC development cost, and time to market while maintaining product quality. At 130-nm, test compression is a must for us in order to meet our quality goals under tight cost constraints. Previously, test compression techniques would have required three weeks of test expertise to achieve our design objectives," said Thomas Ruhnau, manager, Digital Design, Micronas. "DFT Compiler MAX as part of Synopsys' RTL synthesis solution enabled us to achieve 10x test data volume reduction with less than three days of engineering effort while impacting design area by less than one percent. Ease of use, test data volume compression rate and very low area impact on the design are the main driving forces leading to our standardization of DFT Compiler MAX."

"At STMicroelectronics, our test quality requirements are extremely high and can only be achieved on designs at 130-nm and below through the use of DSM fault models. Test compression, therefore, is a must in order to keep test costs at bay," said Stephane Lecomte, DFT engineering manager, Computer Peripherals Group, STMicroelectronics. "With Synopsys' DFT Compiler MAX, we achieved 20x reduction in tester time as part of our synthesis flow with no additional test expertise and no impact on development time. This enabled us to meet our stringent test quality objectives on a recent hard disk drive design. We are standardizing on DFT Compiler MAX for all our new designs."

"Our customers today are facing many demands to produce the highest quality products within the shortest amount of time at the lowest cost," said Antun Domic, sr. vice president and general manager, Implementation Group at Synopsys. "To achieve these requirements, designers need a complete RTL to silicon solution that concurrently optimizes for area, timing, test, power, SI, and yield. With the introduction of DFT Compiler MAX, a new test compression solution in the Galaxy Design Platform, we are now expanding our 1-pass test synthesis technology to address mainstream design. This solution enables our customers to preserve their existing investments in design and test automation tools while achieving high quality results at a lower cost."

Cost and Availability

A one-year technology subscription license of DFT Compiler MAX starts at $120,000. DFT Compiler MAX is offered in limited availability today. A general release expected in September of 2005.

About Micronas

Micronas (SWX Swiss Exchange: MASN; Frankfurt: MNSN; Prime Standard Segment, TecDAX), a semiconductor designer and manufacturer with worldwide operations, is a leading supplier of cutting-edge IC and sensor

system solutions for consumer and automotive electronics. As a market leader in innovative, global TV system solutions, Micronas leverages its expertise into new markets emerging through the digitization of audio and video content. Micronas serves all major consumer brands worldwide, many of them in continuous partnerships seeking joint success. While the holding is headquartered in Zurich (Switzerland), operational headquarters are based in Freiburg (Germany). Currently, the Micronas Group employs about 1900 people. In 2004, it generated CHF 963 million in sales. For more information on Micronas and its products, please visit www.micronas.com.

About Galaxy Design Platform

The Galaxy Design Platform is an open, integrated design implementation platform with best-in class tools and IP, enabling advanced semiconductor design. Anchored by Synopsys' industry-leading semiconductor design tools and the open Milkyway™ database, the Galaxy Design Platform incorporates consistent timing, SI analysis, common libraries, delay calculation, constraints, testability, and physical verification to provide a convergent flow from RTL all the way to silicon. The Galaxy Design Platform helps reduce design time, decrease integration costs and minimize the risks inherent in advanced, complex semiconductor design.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at: http://www.synopsys.com/ .

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