Synopsys Delivers First Complete SystemVerilog Design and Verification Flow

More Than 150 Companies Worldwide Have Adopted Synopsys' SystemVerilog Solutions to Create Today's Hottest Electronics Products

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that it now supports the SystemVerilog language throughout its suite of design and verification products, extending its SystemVerilog leadership and establishing another industry-first achievement. Important elements in Synopsys' comprehensive SystemVerilog design and verification flow were made available today as the company introduced SystemVerilog verification IP support for its VCS® Verification Library in a separate announcement and announced a new native SystemVerilog parser in its Formality® equivalence checker. Design and verification engineers who use logic synthesis, simulation, verification IP, testbench automation, RTL checking, formal analysis and equivalence checking tools can now benefit from the faster performance, improved productivity and increased predictability advantages of using the IEEE Std 1800™-2005 SystemVerilog standard, the industry's only electronic design and verification language.

More than 150 companies are using Synopsys' SystemVerilog solutions today to design and verify the advanced systems-on-chips (SoCs) that are used in cutting-edge consumer electronics, networking and telecommunications equipment and computer systems. Design engineers are able to leverage SystemVerilog to express their highly-complex designs more succinctly and accurately, capture critical design attributes with assertions and develop advanced coverage- driven, constrained-random testbenches. Synopsys products supporting the SystemVerilog standard span the Galaxy™ Design and Discovery™ Verification Platforms. These products include Design Compiler® for logic synthesis, the VCS comprehensive verification solution with Native Testbench, the Pioneer-NTB SystemVerilog testbench automation tool, the Formality® equivalence checker, the Magellan™ hybrid formal analysis tool and the Leda® programmable RTL checker. SystemVerilog support is also provided in the assertion-checker and base-class testbench building-block libraries that ship with Discovery products as well as in the VCS Verification Library.

Leadership in Industry Standards

"Synopsys has been the key driver of SystemVerilog since day one," said Aart de Geus, chairman and chief executive officer at Synopsys, Inc. "We donated key testbench and assertion constructs to the Accellera language standards organization and have continued our industry leadership by working with a wide range of companies to complete the Accellera specification and to achieve IEEE standardization in record time. Throughout this process, we have worked side-by-side with our customers to validate the language in real design and verification environments. The result is a true industry standard that has passed the rigorous IEEE process, has received extensive vendor support and has already been adopted by many users."

Momentum for SystemVerilog continues to grow marked by widespread, mainstream adoption of the language for both design and verification. Leading-edge design and verification engineers began using SystemVerilog during the standardization process and more than 150 Synopsys customers use the language today. With 66 current members in the Synopsys SystemVerilog Catalyst Program, the EDA and IP industry has also lined up behind this standard. Among these vendors, Synopsys continues its leadership; according to a recent ESNUG survey, 79 percent of design and verification engineers using or planning to use SystemVerilog are using Synopsys tools.

SystemVerilog for Design

The SystemVerilog language brings significant productivity benefits to design engineers. Its advanced design constructs yield more compact RTL code, typically a two-to-five times reduction in lines of RTL. Fewer lines of code translate to fewer coding errors and increased designer productivity. The SystemVerilog language also eliminates inconsistent interpretations between simulation and hardware implementation. This clarifies intended design behavior and accelerates equivalence checking. Synopsys' Galaxy Design Platform offers a complete SystemVerilog implementation flow, including Design Compiler for RTL synthesis, Leda for design checking and the Formality equivalence checker. Formality's newly available native SystemVerilog parser eliminates the use of language conversion, improving both accuracy and time to results.

"We are using SystemVerilog in our current projects," stated Ashish Dixit, vice president of Hardware Engineering at Tensilica. "SystemVerilog's features have enabled us to simplify our internal development that in turn allows us to provide greater value to our customers. Moreover, SystemVerilog is easy to adopt since the

language enables us to make incremental changes to our RTL and verification and harness its powers. As an IP provider, we see much potential value with SystemVerilog being the single hardware description language that addresses the needs of both design and verification."

SystemVerilog for Testbench Automation

Coverage-driven, constrained-random testbenches are clearly established as the best method for verifying large, complex semiconductor designs. SystemVerilog is an industry-standard solution with extensive support for constraint specification, model development and identification of functional coverage points. Synopsys' VCS and Pioneer-NTB provide an unparalleled ability to solve complex sets of constraints expressed in SystemVerilog. This allows verification teams to converge on coverage goals more quickly, significantly enhancing productivity while improving design quality.

Successful use of advanced verification techniques requires an effective methodology. The Verification Methodology Manual (VMM) for SystemVerilog, peer reviewed by verification engineers from over 30 semiconductor industry companies and published by Springer Science+Business Media, provides the guidance needed for this success. In its first six months of publication, this book has quickly become an industry best-seller and essential resource. To accelerate the development of VMM-compliant testbenches, Synopsys provides an implementation of the VMM Standard Library of testbench building blocks with VCS, as well as verification IP within the VCS Verification Library.

"After a careful evaluation of available SystemVerilog testbench solutions, we decided to adopt VCS and the VMM to replace our legacy testbench solution," said Dan Abate, principal verification engineer at Mercury Computer Systems, Inc. "VCS provided superior performance and language coverage, enabling us to quickly develop reusable, extensible verification environments using SystemVerilog and the VMM's testbench building blocks such as transaction generators and configurable messaging. SystemVerilog and the VMM methodology also proved easy to learn -- our team was writing production code within two weeks of getting started."

SystemVerilog for Assertions

Although originally focused on use with formal analysis, assertions are now in mainstream use for simulation as well. Assertions capture design intent and enable the use of both simulation and formal methods from Synopsys to check that the RTL design implementation matches this intent. SystemVerilog provides several advantages not available with other assertion languages and methods, including in-line specification within the RTL code, local variables within the assertion statements and a wide range of options for responding to assertion successes or failures.

For more information on Synopsys SystemVerilog solutions, please visit: http://www.synopsys.com/ .

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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