SEQUANS Standardizes on Synopsys VCS, System Studio and Formality Solutions for Verification of Broadband Wireless Access Chips

Synopsys Discovery™ Verification Platform Provides a Complete Verification Solution From System Level Through RTL to Gates

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that SEQUANS Communications, a fabless semiconductor company that develops end-to-end standards-based silicon for broadband wireless access, has adopted key components of the Synopsys Discovery™ Verification Platform to establish a leading-edge chip verification process. Sequans has standardized on the Synopsys VCS® comprehensive RTL verification solution, System Studio for algorithm design and system-level verification and the Formality® formal equivalence checker to ensure consistency between RTL and chip implementations. Sequans has successfully released Base Station and Subscriber Station chips, compliant with the IEEE 802.16-2004 standard. Both chips were developed in record time, and Synopsys' tools helped minimize risks and delays. Sequans plans to soon release its chips for the mobile WiMAX/WiBro market and is using Synopsys tools to help ensure the best time-to-market schedule.

"We selected Synopsys for our verification needs because they provide a complete solution from algorithm design to implementation," said Bertrand Debray, Sequans vice-president of Engineering. "It is important to us that an electronic system-level (ESL) tool for algorithm design and analysis be linked closely with the RTL verification process. Synopsys provides this connection with its well-integrated combination of System Studio and the VCS solutions. In addition, the Formality formal equivalency checking process ensures that our RTL is consistent with our final ASIC implementations."

"Synopsys' Discovery Verification Platform is the industry's leading system, RTL and gate-level verification solution. The VCS solution's integrated high-performance testbench-based verification environment is ideal for verifying complex chips in the rapidly growing WiMAX space," said George Zafiropoulos, vice president of Marketing, Verification Group, Synopsys, Inc. "This integration, when combined with our Reference Verification Methodology (RVM), yields a complete, high-performance process for verifying the industry's largest and most complex chips."

Synopsys Discovery Verification Platform

The Discovery Verification Platform is a unified environment that provides high performance and efficiency of interaction among all platform components, including mixed-HDL simulation, mixed-signal, system-level verification, assertions, DesignWare® verification intellectual property, code coverage, functional coverage, testbenches and formal analysis. Combined with support for industry-standard hardware design and verification languages, including Verilog, VHDL, SystemVerilog, SystemC™ and OpenVera®, and Synopsys' proven Reference Verification Methodology, the Discovery Verification Platform helps designers achieve higher levels of verification productivity by contributing to first-time silicon success within required project cycles.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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