Synopsys Donates Library of Advanced SystemVerilog Assertion Checkers to Accellera Standards Organization

Checkers Proven to Accelerate Customer Adoption of SystemVerilog Assertions to Benefit Entire Industry

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that it has donated a library of advanced SystemVerilog assertion checkers defined in the ARM-Synopsys Verification Methodology Manual (VMM) for SystemVerilog to Accellera, the electronic design automation (EDA) organization focused on EDA standards. Provided as SystemVerilog source code, the checkers included in this library have been widely used by design and verification engineers for the past few years to add SystemVerilog assertions (SVA) to their designs more quickly and more easily, enhancing engineering productivity. In addition, extensive functional coverage information within each checker has provided them with automatic enhancements to existing coverage metrics, fostering a more predictable verification process.

"As the SystemVerilog leader, Synopsys has provided its customers with advanced assertion checkers for several years to enable higher designer productivity and faster adoption of assertion-based verification," said Manoj Gandhi, senior vice president and general manager of the Verification Group at Synopsys, Inc. "Synopsys' donation to Accellera puts these proven checkers on a path to become an industry standard so that even more design and verification teams can achieve similar productivity benefits."

The donated library contains 20 unique assertion checkers, entirely complementary to Accellera's current OVL of assertion monitors. These checkers are used by designers and verification engineers to capture key attributes of their RTL designs. They are easy to use because they correspond directly to widely-used design elements such as arbiters, FIFOs, memories, registers, and handshake interfaces. For example, an engineer can simply connect the "assert_arbiter" checker directly to the request and grant lines of an arbiter, without having to consider which specific assertions and functional coverage points might be appropriate for arbitration logic. This reduces hours or days of effort down to a simple five-minute task to instantiate the checker. These checkers can be used with designs expressed in SystemVerilog, Verilog, VHDL, or mixed-language RTL.

"We are certainly in favor of assertion checkers, as they help SoC designers to complete their verification work more quickly," said Mike Turpin, chair of Accellera's OVL Technical Subcommittee and principal validation engineer at ARM. "Synopsys' donation of these additional checkers to become part of the OVL industry-standard library is to be applauded."

"The success of Accellera's OVL has shown that the industry benefits from a standard library to get 'jump-started' when adding assertions to their designs," said Shrenik Mehta, chairman of the board at Accellera. "This donation will benefit the industry at large, while raising the bar of assertion checkers with valuable coverage capabilities. We are delighted that they have chosen to share their customer-proven library with the rest of the industry through Accellera."

The next meeting of the OVL technical committee will be soliciting user input at the Design Automation Conference (DAC) in San Francisco, CA. The OVL committee is responsible for adding new checkers and incorporating new donations into the OVL standard. Participation in the committee is open to all DAC attendees and interested parties. This event will be held at the Marriott Hotel, Golden Gate Room B2 in San Francisco, CA, on Wednesday, July 26, 2006, from 1:30 p.m. to 3:30 p.m.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com.

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