Synopsys Design Compiler Topographical Technology Accelerates Tapeout of 90nm Multimedia Chip at ETRI

Tight Correlation Between Synthesis and Layout Reduces Time-to-Market

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that the Electronics and Telecommunications Research Institute (ETRI), Korea's leading research and development organization, has used Synopsys Design Compiler® topographical technology to expedite the tapeout of their new 90-nanometer (nm) multimedia chip. The key requirement for this high-performance, low-power video application was achieving the chip's performance targets within a very tight schedule. ETRI designers needed a solution that could reduce the iterations between synthesis and layout while delivering best-in-class quality of results. Using the Design Compiler topographical technology, ETRI achieved their design goals in a single-pass flow with no iterations between synthesis and layout, which significantly reduced turnaround time.

"In the past, we spent too many cycles between synthesis and layout to achieve timing closure," said Mr. S.I. Yeo, principle member of the engineering staff at ETRI. "Topographical technology's tight correlation between synthesis and layout enabled us to meet our performance targets in a predictable, single-pass RTL-to-GDSII flow. As a result, we saved up to three weeks of critical production time on this project."

The Design Compiler topographical technology is an innovative synthesis capability that utilizes Galaxy™ design platform physical implementation technologies to derive interconnect delays. This accurate interconnect delay data allows the Design Compiler tool to predict post-layout design results such as timing, testability and area during synthesis. In addition, the topographical attribute utilizes clock-tree synthesis technology to estimate a design's post-layout power consumption. RTL designers no longer need to wait until layout is complete to uncover critical design issues such as timing violations. This helps eliminate costly iterations required between synthesis and layout to close on design goals and provides a highly predictable RTL-to-GDSII path.

"Synopsys' Design Compiler topographical technology enables customers such as ETRI to bring advanced technology to market faster," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Topographical technology continues to gain momentum with widespread adoption by customers worldwide to achieve the fastest and most predictable path to silicon."

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

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