eInfochips Offers SystemVerilog Migration Services from Legacy Verification Environments

IP-Enabled Services Firm Joins Synopsys' SystemVerilog Catalyst Program

PRNewswire
AHMEDABAD, India and SANTA CLARA, Calif.

eInfochips, Inc., a leading silicon and product design services firm with spec-to-silicon-to-system capabilities, today announced the availability of comprehensive verification migration services to speed the transition from other legacy languages and environments to the widely supported IEEE Std 1800™ SystemVerilog hardware design and verification language. In addition, eInfochips has joined Synopsys' SystemVerilog Catalyst Program and will extend its VeriSuite (http://www.us.design-reuse.com/news/news9183.html) verification package to support SystemVerilog.

eInfochips' SystemVerilog migration services enable companies to easily take advantage of legacy verification environments while adopting the widely supported industry standard SystemVerilog hardware design and verification language. Services include translation of verification components such as bus functional models, bus monitors and random traffic generators; migration of existing test suites; and validation of migrated verification environments. These services take advantage of eInfochips' extensive verification know-how with a wide range of high-level verification languages and methodologies.

"eInfochips and Synopsys have worked together to move customers from legacy environments to a VCS® Native Testbench (NTB) environment for up to five times faster verification performance through Synopsys' VCS NTB Migration Service program," said Steve Smith, senior director of Marketing, Verification Group, Synopsys. "By joining the SystemVerilog Catalyst Program, eInfochips will further enhance its SystemVerilog expertise and help ensure that customers experience the design and verification productivity and quality benefits of SystemVerilog."

"The constantly increasing complexity of SoCs has made verification more challenging," said Pratul Shroff, president and CEO, eInfochips. "With SystemVerilog steadily gaining ground as the next-generation language for verification, we're confident of providing faster and more integrated verification to our customers migrating to the SystemVerilog standard. The SystemVerilog Catalyst Program will enable us to provide enhanced services to our customers in the system-level verification area."

About eInfochips

eInfochips, Inc., based in Santa Clara, is a leading provider of cutting edge ASIC design and verification services, embedded systems solutions and IP cores. Their capabilities extend from Specification to System, with knowledge on ASIC design & verification, physical design, board design and embedded firmware development. The company's India and US design centers have delivered SoC and embedded solutions to a variety of customers thus increasing their cost-effectiveness, reducing their time-to-market and growing their market strength. A partial list of customers includes IDT, Inter Digital, ATI, Agere Systems, Rambus, Texas Instruments, Cypress Semiconductors and Broadcom. For more information on eInfochips, visit www.einfochips.com.

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