Progate Adopts Design Compiler Topographical Technology for Faster Time-to-Results

Topographical Technology Improves Designer Efficiency and Reduces Turnaround Time

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Progate Group Corporation (PGC), one of the largest SoC/ASIC design service providers in Taiwan, has adopted Synopsys' Design Compiler® topographical technology to help accelerate time-to-market for its products. Topographical technology accurately predicts post-layout design performance early in the design cycle, enabling designers to identify and fix issues during RTL synthesis. By eliminating time-consuming iterations between RTL synthesis and physical layout, PGC designers are able to close on their performance goals quickly and more efficiently.

"Topographical technology streamlines the design process by giving our RTL designers visibility into post-layout design issues without having to learn or run physical implementation tools," said Jasper Lee, technical manager at PGC. "The results we have seen using topographical technology correlate within two to six percent of actual layout timing and area. This tight correlation enables our designers to achieve desired performance faster, reducing total design time up to four weeks."

Topographical technology accurately predicts interconnect delays by utilizing Synopsys' physical implementation technologies rather than approximations, also known as wire-load models. In addition, topographical technology incorporates clock-tree synthesis technology to accurately estimate post-layout power consumption. This extends topographical technology correlation beyond timing and area to include leakage and dynamic power.

"Topographical technology continues our strong tradition of bringing to market innovative synthesis technologies," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Design Compiler customers are benefiting from a highly-correlated RTL-to-GDSII flow that significantly reduces their design cycle time and helps them stay competitive in today's market."

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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