Synopsys Introduces Pilot Design Environment

Production-Ready Environment Integrates Proven RTL-to-GDSII Flow With New Utilities to Improve Design Productivity and Tapeout Predictability

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the availability of the Synopsys® Pilot Design Environment, a complete RTL-to-GDSII design system developed by Synopsys Professional Services and based on Synopsys' Galaxy™ and Discovery™ platforms. Synopsys' Pilot Design Environment provides a comprehensive, production-ready design flow with built-in methodologies and utilities to improve designer productivity and accelerate the tape-out of system-on-chip designs. A high degree of automation and configurability enables customers to adapt the environment to meet their project-specific technical and business objectives. In addition, features for capturing and reporting project metrics are integrated into the Pilot Design Environment, enabling customers to monitor and measure project status and better predict achievement of key milestones.

"Synopsys' Pilot Design Environment helped us achieve multiple chip tapeouts at a new technology node in a fraction of the time it would have taken had we built the flow from scratch," said Gary Kirchner, director of Electronic Hardware Design, Honeywell Aerospace. "Utilizing this design environment, we are able to more quickly produce our customers' chips and with lower risk."

Derived from the extensive experience of Synopsys' design services organization and used by Synopsys consultants on dozens of customer design projects each year, the Pilot Design Environment has demonstrated success at improving design productivity and easing significant design transitions, such as migration to a new process node or design methodology. A new graphical user interface (GUI) simplifies setup and configuration of the design flow, technology files and library data, accelerating the design team's time-to-results and easing re-use of the design environment from one project to the next. Since technology and library data is separated from design data, users can quickly re-target the design to an alternate process or library, re-using all or part of the design flow. Separately maintained global and local scripts provide designer-level control of the design flow, enabling designers to modify or tune it to specific project needs.

The Pilot Design Environment is also architected to facilitate multi-site chip development, utilizing a standard data structure that enables geographically-dispersed design teams to work within a common, version-controlled design infrastructure.

"With project members in multiple locations, having a single, uniform design environment is important to help ensure our team stays productive and avoids the problems associated with process and data inconsistencies. The Pilot Design Environment provides that valuable common infrastructure," said Benny Chang, vice president of Engineering at Tundra Semiconductor. "Additionally, the environment is robust and repeatable, allowing us to accommodate late ECOs with minimal schedule impact."

The environment is tapeout-proven at process nodes from 0.25 micron to 65 nanometers. It features implementation and functional verification flows, supporting the Discovery Verification Platform's VCS® Native Testbench and Reference Verification Methodology (RVM), as well as the complete Galaxy Design Platform, including leading tools such as IC Compiler. The environment can be customized to support third-party or customers' internally-developed tools. Advanced methodologies to address deep submicron design issues, such as timing, signal integrity, power, design for test, and design for manufacturing are incorporated into the design flow. Utilities for technology file preparation as well as for qualifying and adjusting library and design data enhance the design team's productivity and help avoid downstream implementation problems by ensuring early and complete node, library and design information.

The Pilot Design Environment is also capable of capturing and reporting approximately 50 design and project-level metrics, providing a means for understanding current project status, evaluating the remaining time and resource requirements, and evaluating the impact to the design of changes to the flow or design data. The ability to consistently monitor design characteristics and resource utilization throughout the development process enables systematic improvements to the design flow. Customers will be able to take advantage of the productivity gains realized in each new release of the Pilot Design Environment.

"With dozens of tapeouts to its credit, the Pilot Design Environment is a validated solution that designers can leverage to achieve tapeouts in a more efficient and predictable manner," said John Chilton, senior vice president and general manager of Synopsys' Solutions Group. "This offering combines Synopsys' unique expertise in tools, design flows, and chip design to help customers avoid common project bottlenecks and more productively focus on their designs and on whole product development."

Pricing and Availability

The Pilot Design Environment is deployed as a service by Synopsys Professional Services and is available now to early adopters. Deployment service fees vary depending on the amount of customization and associated project needs, and include the environment deliverables. An annual support contract is required.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits of the Pilot Design Environment. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties in deploying the Pilot Design Environment for customers, uncertainties attendant to any new technology offering and certain statements contained in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2005 entitled "Management's Discussion and Analysis of Financial Condition and Results of Operations - Factors That May Affect Future Results."

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