# IBM and Chartered Team With Synopsys for Mixed-Signal Connectivity IP at 65 nm

Synopsys USB, PCIe, SATA and XAUI PHYs for High-Volume, Low-Power Applications Available for Foundries' Leading-edge Processes

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that IBM and Chartered Semiconductor Manufacturing have agreed to support Synopsys' DesignWare® Mixed-Signal connectivity intellectual property (IP) on the 65-nanometer (nm) process developed for Common Platform technology. As part of this agreement, Synopsys is porting PHYs for USB 2.0, PCI Express® (PCIe), SATA and XAUI protocols to the 65-nm process technology developed by Chartered, IBM, Infineon Technologies and Samsung, and also porting the DesignWare USB 2.0 nanoPHY IP to IBM and Chartered's 90-nm process node. These PHYs are highly complex process-tuned analog interfaces used in today's high-volume, high-value consumer, computer, storage and networking applications. Availability of this DesignWare PHY IP will give designers access to verified connectivity cores for implementation at 65 nm to help reduce risk, speed time-to-market and ensure a more predictable path to silicon.

Introduced earlier this year, the DesignWare USB 2.0 nanoPHY IP features half the power and die area compared to previous generation solutions. The 90- nm IP silicon has received Hi-Speed USB logo-certification and the 65-nm version is in final development. Synopsys is porting DesignWare PHYs for the popular PCIe, SATA and XAUI protocols to the 65-nm process node to give designer's access to standards-compliant IP with high-value features, such as low power and small area.

"High speed connectivity IP is a critical building block in many of today's leading edge designs. We selected Synopsys because of their expertise in complex mixed-signal connectivity IP and ability to deliver IP in the context of a complete solution," said Steven Longoria, vice president, Semiconductor Technology Platform at IBM Technology Collaborations Solutions. "We are focused on continually expanding the Common Platform technology ecosystem with validated process-aware IP. These PHYs will be available to both our ASIC and foundry clients."

"Our customers require that the Common Platform offers early availability of standardized interface IP for USB, PCIe, SATA and XAUI protocols that can be manufactured with confidence at multiple foundries," said Kevin Meyer, vice president of Worldwide Marketing and Platform Alliances at Chartered. "These high-value cores from Synopsys allow chip designers to quickly obtain and integrate critical functionality into their designs and then ramp into volume production at Chartered or IBM. We are taking an even more aggressive position in making available reduced-risk IP at the leading edge, being among the first companies at 65 nm to have Synopsys port this IP."

"Availability of reliable mixed-signal IP has become central to enable the migration of SoC designs to smaller geometries," said Guri Stark, vice president of Marketing for the Solutions Group at Synopsys. "We've worked closely with IBM and Chartered to deliver these key IP cores to help designers achieve power and area savings in 65-nm and 90-nm chip designs. Combining these PHYs with our other IP offerings and a complete Common Platform technology reference design flow make Synopsys the obvious choice for designers who want to take advantage of the flexibility, reduced risk and cost savings of the Common Platform technology."

Availability

Synopsys' DesignWare USB 2.0 nanoPHY IP is available now for the CMOS 9SF and CMOS 9LP 90-nm processes and in Q3'06 for the CMOS 10LP 65-nm process. PCI Express, SATA and XAUI PHYs are expected be available in Q4 of calendar 2006 for the CMOS 10LP 65-nm process.

About DesignWare Mixed-Signal IP

Synopsys enables designers to quickly integrate analog Mixed-Signal IP (MSIP) into next-generation system-on-chips (SoCs) with a comprehensive portfolio of high-performance PHYs for the PCI Express, SATA, XAUI, and USB protocols. In addition, the MSIP offering also includes a complete suite of I/O Libraries. Available for industry-leading processes, DesignWare Mixed- Signal IP meets the needs of today's high-speed designs for the networking, storage, computing, and consumer electronics markets. The DesignWare MSIP offering is complemented by a comprehensive suite of digital controller cores and verification IP to provide chip developers with a complete solution for SoC integration. Each MSIP can be licensed individually, on a fee-per-project basis or customers can opt for the Volume Purchase Agreement, which enables them to license all the

MSIP in one simple agreement. For more information on DesignWare MSIP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits of IBM and Chartered's support of Synopsys' DesignWare Mixed-Signal connectivity intellectual property (IP) on the foundries' 65-nanometer (nm) process and expected dates of availability of the ported solutions. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties in manufacturing customer designs in a new process technology, uncertainties attendant to any new product offering and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended April 30, 2006 entitled "Management's Discussion and Analysis of Financial Condition and results of Operations -- Factors That May Affect Future results."



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