SGI Adopts Synopsys Design Compiler Topographical Technology for Predictable RTL-to-GDSII Flow

Accurate Prediction of Post-Layout Design Results in Synthesis Enhances Productivity and Accelerates Timing Closure

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Silicon Graphics, Inc. (OTC: SGI), a leader in high-performance computing, has deployed Synopsys' Design Compiler® topographical technology for its next-generation ASIC designs. SGI utilized its next-generation NUMAlink™ testchip as a vehicle to validate the topographical technology for broader deployment within SGI. With its ability to accurately predict post-layout timing and area results in synthesis, topographical technology enables SGI's RTL designers to predict and fix design issues up-front, resulting in significant productivity gains and faster timing closure.

"We have found the topographical technology to be very effective in delivering predictable flows," noted Gary Benzschawel, design manager at SGI. "Using topographical technology our RTL designers were able to identify the design issues and fix them prior to physical implementation. The accuracy and predictability of results combined with the advanced optimizations of Design Compiler technology are what our RTL designers need for synthesis at 90-nm technology."

Part of Design Compiler Ultra, topographical technology brings accurate timing and area context into the synthesis engine, enabling RTL designers to predict potential design issues early in the design cycle rather than waiting for initial physical implementation results. It utilizes Synopsys' advanced physical implementation algorithms to eliminate the need for wire-load model-based approximations in synthesis and generates a better starting point for physical design. By providing a better starting point for physical implementation, topographical technology eliminates costly iterations between synthesis and layout to reduce overall design time.

"Designers worldwide are realizing the tremendous benefits of predictability with topographical technology," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "While Design Compiler continues to offer best-in-class timing, area, power, and test optimization, topographical technology adds the productivity boost required for our customers to stay competitive in today's market and this further validates Synopsys' leadership in bringing innovative synthesis solutions to market."

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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