

Synopsys' coreAssembler Tool Decreases Design Time for Leading Semiconductor Companies by Up to 67 Percent and Significantly Reduces SoC Cost

Tool Enables Designers to Rapidly Configure and Assemble SoCs From Pre-Designed and Packaged IP Blocks

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Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced the general availability of coreAssembler, a tool that has been used by NEC Electronics and National Semiconductor to implement an intellectual property (IP) based flow, which dramatically reduces design time, risk and cost of their advanced system-on-chip (SoC) platforms and ICs. These two companies and others have used coreAssembler to efficiently create configurable, reusable platforms, which they and their customers have then used with coreAssembler to automatically configure and assemble IP-based SoCs into volume production.

The coreAssembler product is part of the complete set of IP reuse tools available from Synopsys, which includes coreBuilder for IP block packaging, coreConsultant for configuration and implementation of individual IP blocks and coreAssembler for the assembly and configuration of IP-based subsystems and complete SoCs.

"coreAssembler enabled us to create market-specific V850E and ARM Powered™ platforms for a range of different applications that are easily configurable and supportable and are well integrated into our manufacturing process," said Yoshikazu Sakurai, Project Manager at NEC Electronics. "By using coreAssembler to capture our system-level integration knowledge and automate the creation, assembly and configuration of our IP and platforms, we are eliminating the costly errors that could occur with the previous manual integration process. This has led directly to a savings of up to 60 percent of the time to develop our SoC subsystems."

"By packaging our IP with coreBuilder and using coreAssembler to assemble and configure the SoC, we have reduced our SoC design time by 67 percent while achieving working silicon," said Martin Embacher, design engineering manager at the Cores Development Group, National Semiconductor. "The tool automated what used to be a purely manual assembly process. coreAssembler reduces risk of chip integration and speeds our time to volume silicon."

"Leading semiconductor vendors such as NEC, National Semiconductor and other companies have standardized their IP-based SoC design flows on our IP Reuse tools, including coreAssembler, and have achieved dramatic improvements in productivity," said John Chilton, senior vice president and general manager, Synopsys Solutions Group. "Integrating larger IP-based subsystems into their designs is a growing need among DesignWare® users, with the general release of coreAssembler many more companies will be able to automate the assembly of IP-based platforms allowing designers to more efficiently build these larger subsystems for their complex SoC designs."

Pricing and Availability

The Synopsys coreAssembler tool is included for no additional charge in the DesignWare Library for use with DesignWare IP; a separately licensed version is available today for \$7,350 on a 1-year term subscription license. The IP packaging tool, coreBuilder is available today for \$88,200 on a 1-year term subscription license. coreConsultant is licensed free-of-charge and also is included with the DesignWare Library.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at <http://www.synopsys.com/>.

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