CreVinn Adopts Synopsys' VCS Native Testbench to Accelerate ASIC Development

VCS Native Testbench Helps CreVinn Speed Testbench Development and Performance to Deliver a Higher Level of Verification

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that CreVinn Teoranta, a developer of networking, automotive and computing ASICs, FPGAs and intellectual property (IP), has adopted Synopsys' VCS® comprehensive RTL verification solution for use in its chip verification methodology. CreVinn is taking advantage of the built-in verification features of the VCS solution, including Native Testbench (NTB) technology, to speed the IC verification process. By natively integrating a comprehensive set of bug-finding technologies, the VCS solution offers up to 5x faster verification performance compared with using stand-alone tools. The VCS solution is a key component of the Discovery™ Verification Platform.

"VCS NTB's advanced language features enable us to cut testbench development time in half compared with our previous C++ techniques," said Vincent Gavin, co-founder and chief technical officer at CreVinn. "VCS NTB lets us work at a higher level of abstraction and provides higher performance, allowing more advanced system-level testing than was previously possible. This productivity improvement is a competitive advantage in our contract work as well as in our in-house product development because it allows us to complete more verification cycles within a fixed schedule."

Native Testbench technology provides every customer of the VCS solution with a full-featured advanced-testbench capability. VCS NTB's powerful constraint-solver delivers higher productivity by automating the generation of constrained-random test stimulus, while functional coverage improves project tracking and predictability by enabling engineers to accurately measure the quality of verification. VCS NTB's support for the object-oriented programming style helps engineers design efficient, reusable testbenches for improved expansion and portability.

"The VCS NTB technology enables a comprehensive verification methodology in a single solution," said Farhad Hayat, vice president of Marketing, Verification Group, Synopsys, Inc. "With full-featured testbench capabilities, as well as built-in assertions and a wide range of coverage metrics, ASIC developers such as CreVinn can complete their projects with a higher level of verification in less time."

Synopsys Discovery Verification Platform

The Discovery Verification Platform is a unified environment that provides high performance and efficiency of interaction among all platform components, including mixed-HDL simulation, mixed-signal, system-level verification, assertions, DesignWare® verification intellectual property, code coverage, functional coverage, testbenches and formal analysis. Combined with support for industry-standard hardware design and verification languages, including Verilog, VHDL, SystemVerilog, SystemC™ and OpenVera®, and Synopsys' proven Reference Verification Methodology, the Discovery Verification Platform helps designers achieve higher levels of verification productivity by contributing to first-time silicon success within required project cycles.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

SOURCE: Synopsys, Inc.

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