Synopsys Demonstrates Low Power, IP, Performance and Yield Innovations at 41st DAC

Company Leads in Convergence of Key Technologies for Design, Verification, IP and DFM

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.

Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, will highlight key innovations at the 41st annual Design Automation Conference (DAC), enabling designers to converge quickly to silicon success. Synopsys will showcase the most complete power management solution in EDA, as well as advances in quality of results, verification complexity and correlation-to-silicon. The company will demonstrate 2X or higher advances in performance, capacity and yield enhancement features recently introduced as part of Galaxy™ 2004. Intellectual property (IP), analog mixed-signal, SystemVerilog and strategies for addressing 90 and 65 nanometer design issues -- including design for manufacturing (DFM) -- will also be shown in the demos and the suites.

"The relationship between technology and economics is impacting designers more than ever as we move to 90- and 65-nanometer design," said Synopsys Chairman and CEO Aart de Geus. "Today's complex SoC designs require the convergence of fully integrated design and verification platforms based on best-in-class tools, DFM technology and a robust portfolio of IP, all backed by expert design services and support. Synopsys is the only EDA company that offers all these elements in a complete concept-to-silicon flow to achieve performance, power and area goals while reducing cost and schedule risk."

Compute power, multi-media, graphics and communications features are converging in consumer products, putting additional pressure on engineers to create designs that are especially sensitive to cost, power consumption and size. Synopsys is addressing these tough challenges with its best-in-class Galaxy™ Design and Discovery™ Verification Platforms, extensive DesignWare® intellectual property (IP) portfolio, design for manufacturing (DFM) solutions and design services.

Synopsys executives and experts will be presenting and participating in more than 30 panels, tutorials and events, covering a broad range of topics, from a basic introduction to EDA, to business issues in EDA and IP, to technical workshops on design, verification, IP and DFM. Synopsys Chairman and CEO Aart de Geus will once again participate in the CEO panel, "EDA: This is Serious Business," as well as in the eighth annual "EDA Business Forum at DAC." Additionally, at the Partner Booth, Synopsys and its strategic partners will show how they are delivering collaborative design solutions from design to manufacturing.

Special Power and Interoperability Events

Synopsys will host a luncheon panel on design-to-silicon power management on Tuesday, June 8 from noon to 2:00 p.m. in meeting room 25A-C of the convention center. The panel will include speakers from leading IP, foundry and EDA companies, and will offer insights into the newest performance-enhancing techniques, including how to optimize system-wide power use and maximize battery life.

For the sixth year in a row, Synopsys will also host an Interoperability Breakfast to encourage designers and suppliers to explore myths about interoperability and share how they are using signal integrity libraries and the SystemVerilog language to design, verify and implement state-of-the-art designs. The event, titled "Myth Busters: Interoperability Languages and Libraries," will take place Wednesday, June 9 from 7:30 to 10:00 a.m. in the Marina Ballrooms E-G of the San Diego Marriott Hotel & Marina.

Registration for these events is available by visiting Synopsys at http://www.synopsys.com/ .

Synopsys at DAC

Visit Synopsys at booth #4825, and at the Partner Booth, #4731. Customers interested in signing up for suite demonstrations are encouraged to register in advance at http://www.synopsys.com/news/events/dac2004/dac2004.html . A detailed listing of seminars, panels and events in which Synopsys will participate is also available via this link.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify

the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

SOURCE: Synopsys, Inc.

CONTACT: Yvette Huygen of Synopsys, Inc., +1-650-584-4547, or yvetteh@synopsys.com; or Andrea Zils of Edelman Public Relations, +1-650-968-4033, or andrea.zils@edelman.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/