New DesignWare Verification IP Alliance Program Expands Availability of High-Quality VMM-Enabled Verification IP

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Alliance Helps Speed Testbench Development; Launches with eInfochips and NoBug

MOUNTAIN VIEW, Calif., Feb. 11 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced the launch of its DesignWare® Verification IP (VIP) Alliance program with initial members eInfochips, a spec-to-system solutions company, and NoBug, a digital design, verification and EDA company. Both are current members of the Synopsys VMM Catalyst Program and have been selected for their depth of experience with verification methodology and verification IP. The Alliance will provide designers with access to a broader range of Verification Methodology Manual (VMM)-enabled verification IP, complementing the Synopsys DesignWare verification IP portfolio. By establishing a network of pre-qualified VIP vendors, Synopsys is helping designers accelerate and simplify the verification of IP blocks in their system-on-chips (SoCs) with less risk and faster time to results.

To help deliver a consistent use-model for designers, the VIP offered by the partners through the DesignWare VIP Alliance will be developed in accordance with the guidelines used by Synopsys' verification IP engineering experts. Furthermore, the members will use Synopsys' internal VIP VMM rating tool, which enables them to ensure the compliance of the Verification IP to the VMM standard. The VMM features included in the Alliance members' VIP provide easy integration into SystemVerilog VMM verification environments, helping to speed testbench development time.

"We have been developing verification IP for many years and have seen wide adoption of VMM as well as an increasing demand for VMM-enabled verification IP," said Sribash Dey, vice president of Sales at eInfochips. "By working closely with Synopsys, our mutual customers can have access to a wider range of VMM-enabled Verification IP that helps accelerate their verification process."

"With such high activity around VMM, it's important to provide designers with verification IP to meet their design requirements," said Moshe Shalev, NoBug's CEO. "As a DesignWare VIP Alliance member with access to the guidelines and VMM rating tool used by Synopsys, we will be able to provide VIP that is complementary to DesignWare VIP and meets the high-quality expectations of our mutual clients."

"The DesignWare VIP Alliance members have gained our confidence through their experience in VMM-enabled verification IP development, and we trust their ability to provide our mutual customers with essential verification IP and services," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "This Alliance enables designers to have easy access to pre-qualified vendors for their Verification IP needs and helps them accelerate the adoption of new technologies into their SoCs with less risk."

Availability

HDMI Verification IP is available immediately through the DesignWare VIP Alliance. For more information on the DesignWare VIP Alliance program visit: http://www.synopsys.com/VIP.

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip designs. As a leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solutions for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. When combined with a robust IP development methodology, extensive investment in quality and comprehensive technical support, DesignWare IP enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About VMM

The VMM methodology enables chip development teams to use SystemVerilog to create comprehensive verification environments using transaction-level, coverage-driven, constrained-random and assertion-based techniques, and specifies library building blocks for interoperable verification components. The VMM methodology has been proven in production by hundreds of SoC and silicon IP verification teams around the world. In addition to the VMM base class library and applications, a variety of useful resources that help improve productivity for both new and existing VMM users are available at http://www.vmmcentral.org.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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