Open-Silicon Uses Synopsys IC Compiler to Achieve 1.3GHz Frequency on Quad-Core ARM Cortex-A9 MPCore Processor

Success Drives Open-Silicon to use Galaxy Implementation Platform for High-Performance Design

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Highlights:

- 1.3 GHz frequency on quad-core ARM® Cortex™-A9 MPCore™ processor
- 5X reduction in number of high power cells
- Correlation within 5% between synthesis and post-route timing drove predictable closure

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that Open-Silicon used Synopsys® IC Compiler™ place and route solution to achieve 1.3 GHz performance on a quad-core ARM Cortex-A9 MPCore processor. IC Compiler is a cornerstone of the Synopsys Galaxy™ Implementation Platform, and its advanced optimization technologies, unique leakage power recovery capability and predictable flow with Synopsys Design Compiler® Graphical synthesis solution were key contributors to Open-Silicon achieving the performance and power targets and predictable timing closure for the hardened processor core.

"We established the Center of Excellence for ARM based designs to provide our customers with complete ARM solutions from ARM sub-system design to power and performance-optimized processor hard macros," said Taher Madraswala, senior vice president of Engineering, Open-Silicon. "For performance optimization, we collaborated with Synopsys to leverage innovative technologies from the Galaxy Platform to enable the 1.3GHz frequency that our customers need to differentiate themselves in the market. As our leading-edge customers continue to push the power/performance envelope, we are confident that the winning combination of our design expertise and Synopsys tools and technologies will enable Open-Silicon to continue to deliver state-of-the-art ARM performance."

The quad-core processor targeted at a set-top box application was a sizeable design totaling more than three million instances with hundreds of macros, including four ARM NEON™ media processing engines. Implemented hierarchically, the design achieved a frequency of 1.3 GHz at the typical corner using 69 percent low-power long channel cells. Open-Silicon optimized the hard macro for a TSMC 40LP low-power process using ARM POP™ IP, comprised of standard cells and memories, as well as Synopsys' high-speed DesignWare® Embedded Memories.

Many factors made timing closure a challenging task:

- Additional levels of logic were introduced by the complexity of the quad-core configuration
- The high cell density required for a compact core amplified timing sensitivity to placement, requiring tighter correlation between synthesis and place and route
- Top-level floorplanning required careful tuning to improve timing and area
- Performance was the highest priority, but leakage power also had to be managed
- The parts of the design related to memory access run at twice the processor clock speed (half clock cycle), further straining timing closure

The Open-Silicon design team created a flow with Design Compiler Graphical and IC Compiler that converged on timing quickly and predictably. They took full advantage of key capabilities such as:

- Design Compiler Graphical's physical guidance for 20 percent improved timing and 5 percent post-route correlation with IC Compiler
- IC Compiler's useful skew technology to close timing on the memory half cycle paths
- IC Compiler's final-stage leakage recovery that delivered a 5X reduction in the number of high power cells without impacting performance

Other Galaxy platform tools used in the quad-core implementation include Formality® for equivalence checking as well as StarRC™ and PrimeTime® for signoff extraction and timing analysis.

"Open-Silicon has a reputation for on-time delivery of complex SoC designs that meet performance and power targets and result in first-pass silicon success," said Dr. Antun Domic, senior vice president and general manager, Implementation Group at Synopsys. "Open Silicon's success in leveraging the differentiating technologies in Design Compiler and IC Compiler to

predictably meet challenging design targets reinforces the position of the Galaxy Implementation Platform as the widespread choice for high-performance design."

Resources

- Synopsys Galaxy Implementation platform
- SNUG 2012 Proceedings: Open-Silicon: Implementation of ARM Cortex-A9 Quad Core Processor with Synopsys Hierarchical Flow

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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