Latest Release of Synplify Software Cuts Days off FPGA Implementation Time

New Features Include Fast Error Identification, Incremental Fix and Customizable Reporting for Faster FPGA Implementation and Prototype Bring-Up

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Highlights:

- New debug flows for multiple error isolation and incremental fix capabilities enable faster implementation of large FPGA designs and FPGA-based prototypes, such as Synopsys' HAPS® systems
- New constraints setup assistance for Xilinx Vivado Design Suite users eases migration to Vivado flow, improves design performance and helps avoid constraints omissions
- Triple modular redundancy and inference of error-correcting code fault-tolerant RAMs has been added for Altera devices
- Support for Achronix Speedster22i HD FPGAs delivers optimized synthesis results

Synopsys, Inc. (Nasdaq:SNPS), a global leader accelerating innovation in the design, verification and manufacture of chips and systems, today announced the latest release of the Synopsys Synplify Pro® and Synplify® Premier FPGA synthesis tools. The 2012.09 Synplify releases include new multiple error isolation and incremental fix capabilities that accelerate FPGA implementation. These features enable FPGA designers and engineers deploying FPGA-based prototypes such as Synopsys' HAPS systems to cut weeks off their design project schedules.

The 2012.09 Synplify Premier release also delivers significant enhancements for engineers targeting Altera and Xilinx FPGAs and, for the first time, includes support for Achronix Speedster 22i HD FPGAs. For engineers targeting Xilinx 7 Series devices, new automated constraints setup assistance and checking for Xilinx's Vivado Design Suite simplifies migration from the Xilinx ISE design software, saving time and enhancing quality of results. For designers targeting Altera FPGAs, the new version of the Synplify Premier tool provides high reliability capabilities, such as triple modular redundancy (TMR) and automatic inference of error-correcting code (ECC) memories. Synplify customers with all-vendor configurations of Synplify Pro and Premier can now target Achronix's Speedster22i HD FPGAs built on Intel's 22nm process technology with 3-D Tri-Gate transistors.

The new hierarchical design error isolation and incremental fix capabilities in the Synplify Premier software, in conjunction with enhanced continue-on-error capability, can significantly shorten design cycles by speeding up design fixes and reducing the number of iterations needed to successfully bring-up the FPGA design on the board. These features, including TCL scripts and clock conversion and error reports, can automatically identify and isolate multiple erroneous modules and interface issues in a single synthesis run. The erroneous modules can now be exported, fixed in parallel with the main design, and then merged back into the design incrementally. In addition, enhancements to the clock conversion feature enable users to create custom reports early in the synthesis run and perform TCL script-based searches of the design database to find converted clocks. This ability to determine whether conversion completed as planned saves designers debug time and is particularly useful when initially bringing up a prototype on a board.

"We have been working closely with Synopsys for over a year to ensure seamless integration between Synplify and the Vivado Design Suite for customers using our 7 series FPGAs," said Tom Feist, senior marketing director of design methodology Xilinx. "In particular, the new constraints setup capability offered in the latest Synplify release has greatly helped our customers accelerate the creation of good design constraints and improve design performance."

Synopsys and Xilinx worked together to provide an integrated RTL-to-gates flow that simplifies the migration path to the Xilinx Vivado Design Suite for designers using Xilinx 7 Series FPGAs. The new flow adopts standard Synopsys Design Constraints (SDC) timing constraints specifications and provides the option to use the Verilog netlist format as the output from synthesis and input to place-and-route. The latest Synplify software also defines a migration path from Xilinx's ISE place-and-route flows to Vivado flows by providing constraints translation, constraints editing, review and reporting within the Synplify tool.

"Altera's FPGAs provide a proven solution for high-reliability applications," said Alex Grbic, director of software and IP marketing at Altera. "The enhanced TMR functionality in Synopsys' Synplify Premier software automatically implements the triplicated logic and associated voting and control mechanisms, providing a complementary solution to our Quartus II software. As a result of our longstanding partnership, customers using Altera devices can take advantage of the new high-reliability features in the Synplify Premier software for use in their mission-critical applications."

The Synplify Premier software's enhanced high-reliability features have been extended to support Altera devices, providing

designers with the ability to create immunity to radiation effects that cause single event upsets (SEUs). In addition to enabling the creation of fault-tolerant sequential logic including state machines, the Synplify Premier software now allows designers to automatically implement error mitigation circuitry including automatically distributed TMR with voting logic, as well as perform automatic inference of Altera error correcting memory primitives.

"As FPGA designs pass the five million gate mark, the need for synthesis tools that provide fast design turnaround and improve productivity is more important than ever," said Ed Bard, senior director of marketing of the Solutions Group at Synopsys. "In addition to improving performance significantly, we enhanced the debug capabilities in the latest releases of Synplify Pro and Synplify Premier to allow multiple error isolation and incremental fix up, addressing the fast turnaround time requirements of designers implementing large-scale FPGAs for production applications or SoC prototyping."

Availability and Resources

The 2012.09 release of the Synplify Pro and Synplify Premier synthesis software is available now. Customers with a current maintenance agreement can download this new version from Synopsys using their SolvNet account. The Synplify FPGA synthesis products are supported on Windows and Linux, 32 and 64-bit platforms.

- Learn more about Synplify Implementation tools:
  - https://www.synopsys.com/FPGAimplementation
  - https://www.synopsys.com/cgi-bin/sld/pdfdla/pdfr1.cgi?file=fpga-debug-10-ways.pdf
- Read about the integration of Synplify Premier with the Xilinx Vivado Design Suite: https://www.synopsys.com/fpga-synplify-xilinx

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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