Synopsys Introduces Memory Test and Repair Solution for Designs at 20 Nanometers and Below

STAR Memory System's New Architecture and Test Algorithms Reduce Test Area up to 30 percent and Increase Coverage for New Memory Defects

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Highlights:

- Optimized memory test and repair algorithms efficiently address new memory defects, including process variation faults and resistive faults, at 20 nanometers (nm) and below
- New hierarchical architecture delivers up to 30 percent reduction in memory test and repair area
- Hierarchical implementation accelerates design cycles by allowing incremental generation, integration and verification of test and repair IP at various design hierarchy levels
- Support for test interfaces of high-performance processor cores enables designers to maximize productivity and system-on-chip (SoC) performance

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced a new release of its DesignWare® STAR Memory System®, an automated pre- and post-silicon memory test, debug, diagnostic and repair solution that enables designers to improve quality of results (QoR), reduce design time, lower test costs and optimize manufacturing yield. The latest release, targeting 20-nm- and FinFET-based designs, includes a new architecture enabling hierarchical implementation and validation of large SoC designs containing thousands of embedded memories, which can decrease the time required to implement tests while also reducing area by as much as 30 percent. In addition, the new release efficiently addresses test and repair for new memory defects seen in 20-nm processes and below such as process variation faults and resistive faults.

"With embedded memories occupying nearly 50 percent of an SoC, having a comprehensive memory test solution with built-in self-test and repair is critical to achieving optimal yield, while lowering overall costs," said Eric Esteve, IP Analyst at IPNest. "Synopsys' introduction of its next generation of the DesignWare STAR Memory System significantly improves designers' ability to detect specific memory defects and failure mechanisms that are prevalent in designs at 20 nanometers and below."

The new architecture in the STAR Memory System provides advanced memory addressing and programmable memory background patterns needed to create optimized test algorithms for detecting not only static and dynamic faults, but also process variation and resistive faults, which are more likely to occur at technology nodes of 20 nm and below. The new version also optimizes the test generation logic by storing only the unique test elements, providing significant area savings.

The STAR Memory System allows hierarchical generation and verification of the test and repair IP within the SoC while maintaining the original design hierarchy. This can speed up design and verification time while allowing reuse of existing design constraints and configuration files, reducing the overall SoC design time. The combination of these new features reduces total test and repair area by up to 30 percent compared to the previous generation product, while enabling faster design closure. These capabilities can also reduce the time required for silicon bring-up and defect analysis for yield optimization, enabling the ramp to volume production to occur in weeks rather than months.

The solution allows at-speed test and repair of high-performance processor cores by using a preconfigured test bus, which provides access to the memories inside the core in test mode. The system uses this bus to test memories and adds memory test and repair logic outside the IP core to avoid any impact on processor core performance. Designed for use with repairable and non-repairable memories for any foundry or process node, the STAR Memory System provides integration with Synopsys' DesignWare Embedded Memories by hardening the timing-critical test and repair logic within the memories, further improving performance, power and area as well as test quality.

In combination with Synopsys' comprehensive portfolio of synthesis-based test solutions including TetraMAX® ATPG and DFTMAX™ compression, DesignWare SerDes IP with built-in self-test and Yield Explorer® tool for yield analysis, the STAR Memory System provides a complete test solution suite to quickly meet overall test cost and quality goals.

"For 20-nanometer SoC designs, implementing robust, area-efficient memory test and repair IP is critical to managing manufacturing yield," said John Koeter, vice president of marketing for IP and systems at Synopsys. "The latest STAR Memory System release not only improves fault coverage and repair, but does so while reducing silicon area by almost a third, enabling engineering teams to get their 20-nanometer designs to market faster with lower manufacturing costs."

Availability and Resources

The DesignWare Star Memory System is available now.

- Learn more about the DesignWare STAR Memory System:
  - https://www.synopsys.com/bist
  - https://www.synopsys.com/designware-ip/memories-logic-libraries.html
- Visit Synopsys booth at ITC for live demo and discussions:http://www.itctestweek.org/
- Learn more about other Synopsys test automation products: https://www.synopsys.com/Tools/Implementation/RTLSynthesis/Test/Pages/default.aspx

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries and configurable processor cores. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to following traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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