# Leading Taiwanese Companies Select Synopsys PrimeTime SI for Signoff

## ASMedia, Generalplus and Socle save weeks in timing closure

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**Highlights**

- Integrated signal integrity (SI) and delay calculation enable more accurate and faster results than add-on third-party solutions
- Signoff-driven engineering change order (ECO) guidance with IC Compiler can reduce timing closure turnaround-time

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that leading consumer and multimedia companies in Taiwan, including ASMedia, Generalplus and Socle, have adopted Synopsys' PrimeTime™ SI tool for static timing analysis (STA) and signal integrity (SI) signoff. One of the key drivers for PrimeTime SI adoption was the easy-to-deploy, signoff-driven ECO guidance technology with tight links to Synopsys' Galaxy ™ Physical Implementation tool and IC Compiler.

"Our previous approach of using PrimeTime for timing and an add-on third-party tool for SI left margin on the table and took longer for timing convergence," said Chi Chang, vice president at ASMedia. "We selected PrimeTime SI because we trust the PrimeTime STA foundation that has signoff accuracy to HSPICE. It streamlined our flow and achieved runtime well within our signoff criteria."

"In an effort to consolidate signoff tools at our global design centers, we evaluated and selected PrimeTime SI because it simplified our signoff flow and enabled a fully signoff-correlated Galaxy solution flow with StarRC and IC Compiler to improve our turnaround-time on high-frequency, low power designs", said Kevin Lee, senior director at Generalplus.

"We adopted PrimeTime SI due to its signoff-driven ECO flow with IC Compiler as it reduced the ECO iterations and sped up the timing closure for our large, complex designs. Socle will be able to more precisely manage project schedule and provide customers with faster time to market. This technology also increases design performance at advanced nodes and enables a more competitive chip design," said Stone Peng, CEO and president at Socle.

PrimeTime SI extends the PrimeTime STA and signoff environment to incorporate crosstalk delay and noise (glitch) analysis and next-generation signoff-driven ECO guidance. PrimeTime ECO uses patent-pending techniques to deliver an extremely fast and scalable ECO solution with tight links to IC Compiler to reduce iterations and deliver a predictable timing closure flow.

"Making timing closure more efficient is critical to designing bigger chips with ever-shrinking schedules," said Robert Hoogenstryd, director of marketing for design analysis and signoff at Synopsys. "By taking advantage of our technology leadership in timing signoff coupled with a highly correlated and integrated physical implementation flow, designers are immediately more productive and can achieve faster timing closure."

**About Synopsys**

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

**Editorial Contacts:**

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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