Synopsys Achieves 100th Design Win with its 28-nm DesignWare® IP

Tens of Millions of Units Shipped and More Than 30 Test Chip Tape-Outs Demonstrates DesignWare IP Robustness

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Highlights:

- Full line of 28-nm DesignWare IP includes PHYs for USB, PCI Express, SATA, HDMI, DDR, MIPI, as well as data converters, audio codecs, embedded memories and logic libraries
- Availability spans four leading foundries and 10 unique processes, enabling designers to choose the IP that meets their specific design requirements
- Designed for SoC robustness with exhaustive simulations, reliability analysis and at-speed electrical characterization across process, voltage and temperature corners
- Optimized for a range of applications including mobile applications processors, multimedia graphics, networking and storage

Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced the 100th design win of its DesignWare IP optimized for 28-nanometer (nm) processes for multiple leading foundries. The silicon-proven 28-nm portfolio consists of widely-used IP including PHYs for USB, PCI Express, SATA, HDMI, DDR, MIPI, as well as data converters, audio codecs, embedded memories and logic libraries, with tens of millions of units shipped. Synopsys' 28-nm DesignWare IP has been thoroughly silicon-characterized across process, voltage and temperature (PVT) variations in both High-K Metal Gate and PolySiON technologies to ensure design robustness. By having taped out more than 30 test chips in more than ten different 28-nm process nodes, with products shipping in volume production, Synopsys provides designers with high-quality DesignWare IP solutions that can be quickly integrated into a range of system-on-chip (SoC) applications such as mobile applications processors, multimedia graphics networking and storage with less risk and effort.

"As an established IP provider, Synopsys has an extensive track record of delivering high-quality IP in leading process nodes," said Michael Chang, chairman of technical board at Global Unichip Corp. (GUC). "Our close collaboration with Synopsys through the years has enabled GUC to successfully incorporate a broad range of proven DesignWare IP in our customers' most advanced SoC designs. Synopsys' 28-nm IP will enable us to deliver next-generation designs for our customers with excellent margin and yield, while meeting power, performance and area requirements."

Advanced process geometries present additional design challenges in SoCs and IP development. At the 28-nm process node, design rules, leakage power and I/O voltages are substantially different than those in 40- and 65-nm processes. To address 28-nm design requirements, Synopsys modified key design aspects of its IP, while adhering to industry protocol specifications and ensuring reliable operation. For example, to meet manufacturing requirements, Synopsys implemented more than twice the number of restrictive design rule checks for its 28-nm IP compared to the 65-nm process and eight times the number of PVT corners for thorough validation. Furthermore, Synopsys employed advanced low-power design methodologies to address low leakage requirements.

Synopsys developed its 28-nm DesignWare embedded memories using statistical design methodologies to address design variability challenges and incorporated multiple power management features including source biasing and dual voltage rails to deliver up to 70 percent leakage power reduction. DesignWare Logic Libraries incorporate multiple threshold voltage and long channel devices to reduce SoC leakage power. In addition, the Logic Libraries are characterized across a wide range of corners, enabling designers to reduce dynamic power through the use of Dynamic Voltage and Frequency Scaling (DVFS) techniques. These features and design techniques enable designers to successfully integrate 28-nm DesignWare IP into their advanced SoC designs to improve performance, power and area results.

"Developing 28-nm IP is not for the faint of heart. Synopsys has invested close to 100 staff-years in designing and verifying our 28-nm DesignWare IP to ensure interoperability and design robustness." said John Koeter, vice president of marketing for IP and systems at Synopsys. "Synopsys' user survey data indicates that approximately 50 percent of our customers' next designs will be implemented in 28-nanometer processes, so it is important that Synopsys provide designers with high-quality 28-nanometer IP in the timeframe they need to gain a competitive advantage."

Availability
The DesignWare PHY IP for USB 3.0, USB 2.0, USB HSIC, DDR3/2, LPDDR3/2, PCIe 2.0, SATA I/II/III, HDMI 1.4, MIPI M-PHY, MIPI D-PHY, as well as embedded memories, logic libraries and data converters (analog-to-digital converters and digital-

to-analog converters) for select 28-nm processes are available now.

The 28-nm DesignWare audio codecs are scheduled to be available to early adopters in Q4 of 2012.

About DesignWare IP
Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: https://www.synopsys.com/designware.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com.

Forward Looking Statements
This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected availability of Synopsys' 28-nm DesignWare audio codecs. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen production or delivery delays, failure to perform as expected, product errors or defects and other risks detailed in Synopsys' filings with the U.S. Securities and Exchange Commission, including those described in the "Risk Factors" section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended April 30, 2012.

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