Synopsys' DesignWare IP for PCI Express with Support for Low-Power Sub-States Successfully Taped Out in Multiple Designs

Industry-First Support for New PCIe L1 Sub-States Reduces Power Consumption

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Highlights:

- Synopsys is the first IP provider to offer new "off" and "snooze" power states (L1 sub-states) in PCI Express® controller IP
- Ten customer designs have integrated Synopsys' new PCI Express IP with L1 sub-states into camera, card reader, networking and wireless applications, with multiple product tapeouts
- L1 sub-state implementation can reduce PCI Express standby power consumption by approximately 99 percent

Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that its industry-first PCI Express controller IP with support for low-power sub-states has successfully taped out in multiple designs. The addition of the L1.1 ("snooze") and L1.2 ("off") sub-states to Synopsys' DesignWare® controller IP for PCI Express 1.0, 2.0 and 3.0 enables designers to reduce power consumption in key market segments, including camera, card reader, networking and wireless applications serving the ultrabook and tablet markets. L1 sub-states reduce a PCI Express system's link idle power consumption from 15 to 20 milliwatts per lane to 10 microwatts per lane, or by approximately 99 percent, by repurposing the signals between the PHY and the controller so that they turn off the high-speed circuits in the PHY when not in use.

"Reducing power consumption in every aspect of an SoC is key for a mobile design's success," said Eric Esteve, market analyst at IPnest. "The availability of L1 sub-states in PCI Express controller IP will enable lower power consumption, which in turn improves battery life—a key differentiator in today's mobile designs."

Reducing standby power is a prerequisite for the emerging thin and light form factor mobile markets, and has now become critical in multiple market segments that must meet stringent regulatory power requirements such as European Regulation 1275/2008. To address these requirements, PCI-SIG members, including Synopsys, are proposing L1 sub-states to supplement previously adopted power saving features such as Latency Tolerance Reporting (LTR) and Optimized Buffer Flush/Fill (OBFF). Synopsys' first-to-market support for L1 sub-states has already enabled market leaders to integrate this new power-saving technology into ten designs while maintaining backward compatibility with existing PCI Express devices. With first silicon back on several of these designs, adopters are well on their way to delivering their low-power mobile products on or ahead of schedule.

"With the availability of L1 sub-states in our DesignWare controller IP for PCI Express, Synopsys leads the industry in adopting and rolling out the latest PCI-SIG enhancements," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Our complete PCI Express controller IP portfolio helps reduce designers' integration risk and development time. With our first-to-market rollout of L1 sub-states, the portfolio continues to be on the forefront of power conservation for mobile and consumer device designers using PCI Express."

Availability
Synopsys® DesignWare controller IP for PCI Express with support for L1 sub-states is available now. For more information, please visit https://www.synopsys.com/pcie. The L1 sub-state engineering change request (ECR) is in the final stages of becoming an engineering change notification (ECN) to the PCI Express specification.

About DesignWare IP
Synopsys is a leading provider of high-quality, silicon-proven IP solutions for system-on-chip (SoC) designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables

designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com.

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