Synopsys Design Implementation Tools Receive TSMC 20nm Phase I Certification

MOUNTAIN VIEW, Calif., May 31, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that TSMC has given Phase I Certification to Synopsys design implementation tools for its 20-nm process. TSMC certified the tools for its 20-nm design rule manuals (DRMs) and SPICE models. Certified products include Synopsys' IC Compiler™ for physical design; IC Validator for DRC and LVS; StarRC™ for extraction; and Galaxy Custom Designer® for custom implementation. Certification of PrimeTime® for static timing analysis is in progress. Certification covers all the relevant 20-nm technology files including routing rules, verification runsets, extraction rundecks and Interoperable Process Design Kit (iPDK).

Synopsys' Galaxy Implementation Platform features comprehensive support for TSMC's latest set of 20-nm design rules. TSMC has certified a full suite of Synopsys implementation tools, including:

- **IC Compiler:** Innovative-patterning compliant placement, and correct-by-construction innovative-patterning-clean routing help provide the optimal area and performance that can be reliably decomposed during manufacturing
- **IC Validator:** New, native graph-based coloring ensures layout decomposition and in-design integration with IC Compiler for accurate, scalable signoff of 20-nm designs
- **PrimeTime:** Support for multi-valued SPEF model variation impact on timing due to innovative patterning
- **StarRC:** Parasitic variation modeling solution addresses the effects of innovative patterning technology due to mask misalignment and other critical technology requirements
- **Custom Designer:** Productivity aids, such as connectivity assisted editing, with support for new local interconnect and cut poly, 20-nm constraints, and correct-by-construction variable size via creation help manage design-rule complexity

"With TSMC we are addressing the next-generation needs of the design community," said Bijan Kiani, vice president of product marketing at Synopsys. "Design ecosystem readiness for TSMC's 20-nm process requires enhancements throughout the entire design implementation flow."

"Collaborating with Synopsys on TSMC's 20-nm process helps ensure design teams will have the technologies and efficient support needed to address new challenges," said Suk Lee, senior director of Design Infrastructure Marketing at TSMC. "The certified tools from TSMC's Open Innovation Platform and its ecosystem members enable designers to create innovative products that meet their aggressive power, performance and area targets."

Details of Synopsys' 20-nm portfolio can be found atwww.synopsys.com/20nm

About Synopsys®

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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