Synopsys Extends HAPS Debug Visibility by 100X

New HAPS Deep Trace Debug Dramatically Increases Signal Tracing Capacity in FPGA-Based Prototypes

MOUNTAIN VIEW, Calif., April 25, 2012 /PRNewswire/ --

Highlights

- Combination of new Synopsys HAPS hardware and Identify software enables greater visibility of internal signals in FPGA-based prototypes to accelerate SoC design debug
- New release provides approximately 100X more storage capacity for signal traces with sample speeds up to 60 MHz
- Utilization of FPGA memory resources significantly reduced to better accommodate complex SoC prototyping projects

Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced the release of a new Deep Trace Debug feature for users of its HAPS® FPGA-based prototyping systems. With HAPS Deep Trace Debug, prototypers can take advantage of approximately 100 times more signal storage capacity than the traditional memory storage employed by on-chip FPGA logic debuggers. The new Deep Trace Debug feature enhances both capacity and fault isolation capabilities while freeing up the on-chip FPGA memory required for validating complex system-on-chip (SoC) designs.

"The Qualcomm Atheros' Wi-Fi/Bluetooth combo products use leading-edge Wi-Fi standards to achieve Gigabit-per-second throughput, requiring advanced hardware-software validation techniques like those available in Synopsys' HAPS systems," said Manoj Unnikrishnan, director of engineering at Qualcomm Atheros. "Our traditional approach required multiple runs with a lot of trial and error. The high-capacity sample storage available with HAPS Deep Trace Debug allows us to quickly identify bugs and speed full system validation. In addition, HAPS Deep Trace Debug will help us improve state machine coverage, prototyping coverage, and test pattern generation."

Confirming correct functionality of high-speed interface designs often requires sampling at dozens of frequencies for several milliseconds at a time. Traditionally, designers have had to make a choice between capturing long signal trace histories that consume extensive FPGA memory resources or saving FPGA memory resources but losing detailed visibility into signal trace history. By pairing the Synopsys® Identify® Intelligent Integrated Circuit Emulator (IICE™) with a HAPS Deep Trace Debug SRAM daughter board, HAPS Deep Trace Debug allows many unique signal probes with complex triggers to be recorded and provides deeper memory to store extensive state history as the system executes. The SRAM daughter board also frees up the FPGA's on-chip RAM for prototyping an SoC design's memory blocks.

"The GSI Technology NBTSRAM designed onto the HAPS Deep Trace Debug SRAM daughter board enables designers to make the best use of HAPS' interconnect bus bandwidth when performance of the SoC prototype is a high priority," said David Chapman, vice president of marketing and applications engineering at GSI Technology. "Our SRAM devices provide both pipeline and flow-through operation to provide the SoC prototyper the flexibility to choose between fast read memory response and maximum clock frequency. The combination of the GSI NBT SRAM family and Synopsys' Deep Trace Debug feature enables engineers to use their HAPS systems for SoC memory IP hosting or as an extended debug trace buffer."

"With the increased hardware and software complexity of SoCs, designers require advanced debug tools to improve the robustness of their system validation process and facilitate early software development," said John Koeter, vice president of marketing for IP and systems at Synopsys. "HAPS Deep Trace Debug represents an important productivity improvement for debugging complex SoCs by enabling prototypers to capture the long signal trace history needed to identify the root cause of design bugs."

Availability & Resources

HAPS Deep Trace Debug support in Synopsys'Identify RTL debugger software and HAPS Deep Trace Debug SRAM daughter boards is available immediately. For more information, please visit: https://www.synopsys.com/HAPS.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys

is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com.

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