

# Yamaha Standardizes on Synopsys' Processor Designer after Cutting DSP Development Time in Half

Processor Designer Doubles Functionality for XMP-1 Sound Generator Device while Reducing Development Cost

MOUNTAIN VIEW, Calif., Jan. 25, 2012 [PRNewswire/](#) -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that Yamaha has adopted the Synopsys [Processor Designer™](#) tool for the development of its custom-designed digital signal processing (DSP) devices. Using the Processor Designer tool to automate the design and implementation of its XMP-1 DSP, Yamaha doubled the number of sound channels for their high definition sound generator device and taped out six months, or 50 percent, earlier compared to their previous generation device. The design team cited the Processor Designer tool's complete flow, including the generation of an assembler, linker, C-Compiler and instruction-set simulator (ISS), easy-to-use processor description language and optimized RTL output as the differentiating reasons for choosing the tool.

"XMP-1 delivers 32-channel phrase sound generation, AudioEngine™ rich sound effects and LED direct control functionality for amusement or digital consumer applications – a level of functionality not possible with fixed hardware. Processor Designer made the DSP development process easier to attain higher quality," said Morito Morishima, department manager of product development for the semiconductor division at Yamaha Corporation. "With Processor Designer, we doubled functionality for our high definition sound generation DSP, developing it in just one year, including the entire software development tool chain, while reducing cost."

Yamaha's design team found the LISA processor description language of the Synopsys Processor Designer tool easy to use, helping reduce development time by more than 50 percent versus traditional methods. In addition to doubling the number of sound channels in the XMP-1, Yamaha designers were able to reduce the device's silicon size by 20 percent. The added flexibility of a software-based solution enabled the design team to add new algorithms after initial design completion without compromising quality or extending the design schedule. Processor Designer's generated C-Compiler was a key benefit as well. Given the small size of the project's engineering team and limited schedule, manually developing a C-Compiler would have been nearly impossible.

"Increasingly, companies like Yamaha find that fixed hardware does not provide the flexibility they need to optimize functionality, performance and power for their specific application," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Processor Designer offers not only flexibility through software programmability, but also a highly automated flow that produces the RTL design as well as the software development environment. Yamaha's results demonstrate that designers can achieve the optimal design tradeoffs with reduced risk and development cost."

[Processor Designer](#) accelerates the design of both application-specific processors (ASIPs) and programmable accelerators through automated software development tools (assembler, linker, debugger, C-compiler), RTL and instruction set simulator (ISS) generation from a single, high-level specification. ASIPs and programmable accelerators are increasingly essential to support the convergence of multiple functionalities on a single system-on-chip (SoC). This makes them ideal for use in a wide variety of applications including video, audio, security, networking, baseband, control and industrial automation applications.

## About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <http://www.synopsys.com>.

## Editorial Contacts:

Sheryl Gulizia  
Synopsys, Inc.  
650-584-8635  
[sgulizia@synopsys.com](mailto:sgulizia@synopsys.com)

Stephen Brennan

MCA, Inc.  
650-968-8900, ext.114  
[sbrennan@mcapr.com](mailto:sbrennan@mcapr.com)

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