UMC and Synopsys Collaborate to Develop DesignWare IP for 28-nanometer Technology

Collaboration on Embedded Memory and Logic Library for UMC's Enhanced Poly SiON HLP Process Enables Creation of High-Performance, Low-Power SoCs

Hsinchu, Taiwan and Mountain View, California, October 12, 2011 -- United Microelectronics Corporation (UMC) (NYSE: UMC; TWSE: 2303), a leading global semiconductor foundry, and Synopsys, Inc., (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced an expanded collaboration to develop DesignWare® IP for UMC's 28-nanometer(nm) HLP Poly SiON process. Extending its previous successes in UMC's 40-nm and 55-nm processes, Synopsys plans to implement its proven DesignWare Embedded Memories and Logic Libraries in UMC's 28HLP Poly SiON process technology. This collaboration will enable designers to create high-speed, low-power system-on-chips (SoCs) with less risk and improved time-to-market. The longstanding relationship between the two companies extends the availability of high-quality DesignWare IP for a wide range of UMC processes from 180-nm to 28-nm.

While preserving the cost-competitiveness of conventional Poly SiON gate stack and using proprietary process techniques, UMC's 28HLP process technology delivers exceptional performance-to-cost ratio with vastly improved performance and power consumption over other 28-nm Poly SiON industry offerings. This enhanced 28-nm Poly-SiON process provides a natural migration path from 40-nm, enabling easy design adoption and fast time-to-market.

"UMC and Synopsys' close collaboration has spanned many years and technology generations," said S. C. Chien, UMC vice president of Customer Engineering & IP Development Design Support Divisions. "Extending our relationship with Synopsys, a leading and trusted IP provider, into the 28-nm process shows our mutual commitment to helping customers develop their increasingly complex SoC designs. We look forward to bringing these next-generation products to market with our customers."

Synopsys' broad portfolios of embedded memories and standard cell libraries are optimized for speed, power and area and have been silicon proven in more than one billion chips. The DesignWare Embedded Memories and Logic Libraries include advanced power management features such as light-sleep, deep-sleep and shut-down as well as a Power Optimization Kit to help extend battery life in mobile applications. In addition, Synopsys' integrated STAR Memory System® test and repair solution enables designers to achieve higher test quality and yield for their embedded memories while lowering overall chip area.

"Synopsys' collaboration with UMC, a leading foundry provider, will help our mutual customers differentiate their SoC designs with IP that is proven in UMC's robust 28-nm process technology," said John Koeter, vice president of marketing for IP & systems at Synopsys. "Our extensive track record of delivering high-quality IP in advanced nodes gives designers confidence that they can integrate DesignWare IP into their SoCs with less risk and achieve a predictable path to first-pass silicon success."

Availability

The DesignWare Embedded Memories and Logic Libraries supporting UMC's 28HLP process are scheduled to be available in Q2 2012. The 28HLP DesignWare Embedded Memories and Logic Libraries will be available at no cost to qualified licensees as part of Synopsys' Foundry Sponsored IP program.

UMC's 28-nm Poly SiON technology is available for customer pilot production now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and Verification IP for widely used protocols,analog IP, embedded memories, logic libraries and configurable processor cores. In addition, Synopsys offersSystemC™ transaction-level models to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, reuse tools, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter athttp://twitter.com/designware_ip.

About UMC

UMC (NYSE: UMC, TSE: 2303) is a leading global semiconductor foundry that provides advanced technology and manufacturing services for applications spanning every major sector of the IC industry. UMC's customer-driven foundry solutions allow chip designers to leverage the strength of the company's leading-edge processes, which include production proven 40nm, mixed signal/RFCMOS, and a wide range of specialty technologies. Production is supported through 10 wafer manufacturing facilities that include two advanced 300mm fabs; Fab 12A in Taiwan and Singapore-based Fab 12i are both in volume production for a variety of customer products. The company employs over 13,000 people worldwide and has offices in Taiwan, Japan, Singapore, Europe, and the United States. UMC can be found on the web at http://www.umc.com

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the outcome of the collaboration between Synopsys and UMC, the implementation of Synopsys IP on UMC's 28-nm process technology, reduced risk and improved time to market resulting from such implementation, and expected availability and pricing for such implementation. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen production or delivery delays, failure to perform as expected, product errors or defects and other risks detailed in Synopsys' filings with the U.S. Securities and Exchange Commission, including those described in the "Risk Factors" section of the latest Quarterly Report on Form 10-Q for the fiscal quarter ended July 31, 2011.

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