Synopsys Announces Critical Milestone in 20-nm Design Enablement Collaboration With Samsung Electronics

Samsung Successfully Tapes Out First 20-nm Test Chip Using IC Compiler and In-Design Physical Verification with IC Validator

MOUNTAIN VIEW, Calif., July 11, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced that its design enablement collaboration with Samsung Electronics, Co., Ltd., a global leader in advanced semiconductor solutions, has achieved a critical milestone with the successful tapeout of the first 20-nanometer (nm) test chip based on Samsung's High-k metal gate (HKMG) process technology. The test chip was implemented using Synopsys' Galaxy™ Implementation Platform, including the Design Compiler® synthesis, IC Compiler place-and-route, In-Design physical verification with IC Validator, StarRC™ extraction and PrimeTime® signoff tools.

The 20-nm tapeout represents the outcome of early R&D collaboration between Samsung and Synopsys aimed at developing and validating a comprehensive design implementation infrastructure for the next generation of 20-nm gigascale integrated circuits (ICs). Key 20-nm design enablement innovations developed as part of the collaboration include modeling of new device structures, double-patterning-aware place-and-route and In-Design physical verification technology, and coding of advanced routing and design rule checking (DRC). Together, these innovations enable fast routing throughput while delivering full compliance with thousands of complex rules and manufacturable routing patterns.

"Leveraging its deep know-how in advanced process and design technologies, as well as its long-standing partnership with ISDA, Samsung is quickly readying its 20-nanometer solution," said Dr. Kyu-Myung Choi, vice president of System LSI infrastructure design center, Device Solutions, Samsung Electronics. "We are collaborating closely with Synopsys to enable the timely availability of innovative components in our 20-nanometer design infrastructure. Synopsys' technology leadership enabled us to quickly implement and validate our first 20-nanometer test chip. The successful tapeout of this test chip marks a critical milestone towards design readiness for our 20-nanometer process technology."

"Samsung has long been a valued partner who has actively worked with Synopsys on new technology development" said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "This achievement in 20-nanometer design enablement is an example of our early and close collaboration, and demonstrates that we can provide innovative EDA solutions at the right time to meet the design needs of the 20-nanometer process technology. We are committed to continuing our collaboration with Samsung so we can ensure our mutual customers have the necessary infrastructure to successfully design products at today's most advanced technology process node."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/**.**

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding Synopsys' anticipated ability to timely enable the design and validation of 20 nanometer process technology in the future. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, technical or other difficulties in enabling 20 nanometer solutions, design delays, specific customer configurations and other risks as identified in Synopsys' filings with the U.S. Securities and Exchange Commission, including those described in the "Risk Factors" section of the latest Quarterly Report on Form 10-Q for the fiscal quarter ended April 30, 2011.

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