Synopsys Custom Design Solution Enables Moortec Semiconductor to Tape Out High-performance Analog IP

Unified Solution Streamlines Development of Embedded Temperature Sensor IP for 65nm, 40nm and 28nm Geometries

MOUNTAIN VIEW, Calif., June 13, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Moortec Semiconductor Ltd., a mixed-signal IP and semiconductor integrated circuit (IC) provider, has taped out its high-performance analog IP on TSMC's 40LP and 28HP processes using Synopsys' custom design solution and TSMC's interoperable process design kits (iPDKs). The CMOS embedded temperature sensor IP is a complex, high-precision analog design for thermal management applications in advanced-geometry, high-gate-count digital ICs. Moortec used Synopsys' comprehensive custom solution, including the Galaxy Custom Designer® schematic and layout editor, HSPICE® and CustomSim™ circuit simulators, IC Validator/Hercules™ design rule checking and layout versus schematic (DRC/LVS) and StarRC™ extraction tools.

"With shrinking silicon geometries, there is a growing need for on-chip temperature monitoring to increase IC longevity and optimize performance. It is important for us to quickly and reliably develop our temperature sensor IP across multiple process nodes to meet the increased demand," said Stephen Crosher, managing director of Moortec Semiconductor. "We chose Synopsys' custom solution because its advanced capabilities and streamlined integration provides the productivity and performance that our engineers need to quickly design and port the IP between 65-nanometer, 40-nanometer and 28-nanometer nodes while maintaining the accuracy and integrity of the design."

Moortec Semiconductor's latest temperature sensor IP blocks were designed using standard logic processes for 65-nanometer (nm), 40-nm and 28-nm geometries and can be easily instantiated multiple times across systems-on-chips (SoCs) for temperature profiling. Moortec used Synopsys' Custom Designer solution to complete the schematic design and layout for custom analog blocks, the HSPICE circuit simulator for pre-layout simulations and the CustomSim FastSPICE simulator to verify the extracted netlists from the StarRC extraction tool. The design was successfully taped out after final verification signoff with IC Validator for DRC and LVS.

"Synopsys' custom solution continues to build momentum both in terms of customer adoption and technology innovation due to its open environment, integration within the Galaxy Implementation Platform and foundry iPDK support," said Bijan Kiani, vice president of product marketing at Synopsys. "Customers like Moortec Semiconductor are realizing higher productivity in creating complex analog designs at advanced geometries by adopting Synopsys' unified solution for analog and mixed-signal design."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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