Synopsys Collaborates With STMicroelectronics to Help Achieve Critical Milestone in 20-nm Design

ST Successfully Tapes Out First 20-nm Test Chip

MOUNTAIN VIEW, Calif., June 2, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced its close cooperation with STMicroelectronics (ST) in the successful tapeout of ST's first 20-nanometer (nm) technology demonstrator test chip. This tapeout represents a critical milestone in the R&D collaboration between the two companies to develop a comprehensive design enablement solution for system-on-chip (SoC) integrated circuits (ICs) using ST's next-generation 20-nm process technology, co-developed with its ISDA (International Semiconductor Development Alliance) partners in Fishkill, NY.

R&D teams from both ST and Synopsys worked together over the last year to build the foundations of the 20-nm design environment, collaborating in several areas spanning from standard-cell library routability optimization, coding of complex routing, parasitic extraction, and design rule checking (DRC) rules.

"As a joint development partner of the ISDA alliance, STMicroelectronics is at the forefront of advanced process technology development," said Philippe Magarshack, group vice president at STMicroelectronics Technology Research and Development (R&D). "From the onset, we have worked closely with Synopsys to enable the readiness of key components in our 20-nanometer design flow. Synopsys' technology leadership and our close R&D interaction enabled us to validate and optimize the implementation solution. The successful tapeout of our first technology demonstrator chip marks a key milestone towards 20-nanometer readiness. Silicon is expected in Q2 2011."

"STMicroelectronics has been a valued partner for a long time, actively collaborating in new technology development," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "The latest achievements in 20-nanometer design enablement show our close collaboration bearing fruit, and prove we can provide critical components at the right time to meet the 20-nanometer transition needs. We will continue collaborating with ST to achieve a production-ready environment for high-quality 20-nanometer design implementation. As part of this effort, Synopsys will further strengthen its R&D presence in France. Our European R&D team already exceeds 400 engineers across 15 countries."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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