Synopsys and TSMC Collaborate to Deliver Custom Design Solution for 28nm Analog/Mixed-Signal Reference Flow 2.0

Synopsys Galaxy Custom Designer Provides New Capabilities to Address Advanced Process Node Design Challenges

Highlights:

- Parasitic-aware capability reduces the number of late-stage design and layout iterations

- The Layout Dependent Effect (LDE)-aware capability helps to shrink long layout cycles caused by unexpected device interactions

MOUNTAIN VIEW, Calif., June 2, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that it has collaborated with TSMC to deliver Synopsys' custom design solution for TSMC's 28-nanometer (nm) Analog/Mixed-Signal (AMS) Reference Flow 2.0. Part of TSMC's comprehensive 28nm design infrastructure, the flow delivers new advanced automation capabilities to improve productivity and shorten the design cycle. The new capabilities include both parasitic-aware and Layout Dependent Effect (LDE)-aware design methodologies.

"The AMS Reference Flow 2.0 delivers new analog/mixed-signal design automation capabilities for advanced process nodes," said Suk Lee, director of design infrastructure marketing at TSMC. "Custom Designer's environment provides a platform for rapidly developing new design capabilities and integrating TSMC advanced process technology."

Synopsys' comprehensive custom solution was validated for TSMC's AMS Reference Flow 2.0 to help ensure that customers can be more confident in meeting their design quality and timeline requirements. Key components of the solution are Galaxy Custom Designer® custom implementation, HSPICE® circuit simulation, CustomSim™ FastSPICE circuit simulation, Custom WaveView waveform analyzer, IC Validator physical verification and StarRC™ Custom parasitic extraction.

"By collaborating with TSMC, we help ensure that our mutual customers have access to a proven and productive custom IC design solution that has been verified by both companies to address 28-nanometer design challenges," said Bijan Kiani, vice president of product marketing at Synopsys. "The combination of TSMC's and Synopsys' respective expertise in process technology and design automations helps to more rapidly deliver innovative solutions to the marketplace."

Parasitic Aware

The parasitic-aware flow reduces the number of late-stage design and layout iterations due to parasitic effects by accurately estimating pre-layout interconnect parasitics using process-based models. Additionally, interconnect parasitic constraints can also be specified in the schematic and then automatically verified in the layout. "What-if" analysis on completed layouts is also supported. This capability enables designers to easily analyze the effects of transistor parameter changes without modifying the layout and taking into account the actual layout interconnect parasitics.

LDE Aware

The LDE-aware capability helps accelerate the layout process by reducing design iterations to accommodate LDE. This method allows designers to model the layout-dependent effects during the initial pre-layout design phase and accelerate time-to-tapeout.

DAC 2011 Demonstrations

Synopsys will demonstrate Custom Designer with the TSMC AMS Reference Flow 2.0 in several locations at DAC 2011, which takes place in San Diego, Calif. from June 5 through June 8:

- Synopsys Booth #3422: Monday through Wednesday at 4:00 p.m.
- TSMC Booth #2648: Tuesday and Wednesday from 9:00 a.m. to 1:30 p.m.
- TSMC Theater presentation (Booth #2648): Wednesday at 5:00 p.m.

In addition, TSMC will present information on the AMS Reference Flow in The Standards Booth (#3328) on Tuesday from 9:00 a.m. to 12:00 noon.

To register to attend Synopsys technical demonstrations and special events at DAC 2011, please visit the Synopsys at DAC web site.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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