Synopsys DesignWare ARC Sound IP Solution First to Support the Dynamic Resolution Adaptation Audio Standard

DesignWare ARC Sound DRA Decoder Supports the Chinese National High-Definition Audio Standard and Enables an Enhanced, High-Quality Audio Experience

Disclaimer: GlobalFoundries acquired the Synopsys Processor Solutions business on June 1, 2026. Clickhere to learn more.

MOUNTAIN VIEW, Calif., May 11, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the availability of an optimized version of the Dynamic Resolution Adaptation (DRA) decoder software for the widely used DesignWare® ARC™ Sound AS211SFX and AS221BD audio processors. The DesignWare ARC Sound DRA decoder supports the Chinese National HD audio standard that is included in the Blu-ray™ Disc specification and is the first optimized implementation available as part of a comprehensive, commercial audio IP solution. The highly efficient AS211SFX and AS221BD audio processors require 18 MHz to run the optimized DRA decoder for Chinese Digital Broadcast (2.1 channel) and only 134 MHz for Blu-ray Disc (7.1 channel). The DesignWare ARC Sound DRA codec together with the DesignWare ARC Sound audio processors enable original equipment manufacturers (OEMs) and system-on-chip (SoC) designers to deliver an enhanced, high-quality, high-definition audio experience in a wide variety of applications used in Chinese digital broadcasting, digital home theater systems, internet streaming and personal media players.

"As a leading manufacturer of high-definition multimedia solutions for automotive applications, it is essential that we are able to easily integrate IP into our designs to address the needs of emerging applications," said Christian Schwarz, project manager of Hirschmann Car Communication GmbH. "By leveraging Synopsys' DesignWare ARC Sound processors and optimized DRA decoder in our latest premium automotive TV receiver, we were able to extend our device's audio capabilities to support the domestic Chinese CMMB radio services."

"As the authorized certification body for the DRA audio standard, we recognize Synopsys' thorough understanding of this unique audio specification," said Nan Deng, Technology Development Director at Digital Wave Co., Ltd. "By providing an optimized version of the DRA codec that runs on the DesignWare ARC Sound AS211SFX and AS221BD audio processors, Synopsys enables OEMs and SoC designers to deliver HD audio for Chinese consumer electronic products."

Synopsys' DesignWare ARC Sound IP solution is designed by a unique combination of both processor architects and audio engineering professionals to deliver an undeniably high-quality listening experience. The single core AS211SFX audio processor incorporates a powerful dual-MAC DSP optimized for audio processing that minimizes the bandwidth and power consumption needed to support the full range of audio applications. The DesignWare ARC Sound AS221BD dual-core audio processor is optimized for HD audio SoCs targeting Blu-ray Disc and High Definition, Multi-Channel digital audio streaming applications. These highly configurable audio processors are easily integrated and can be optimized for each instance on an SoC. The DesignWare ARC Sound solution also includes a media software framework that provides a unified software interface to the extensive library of DesignWare ARC Sound audio codecs and audio post-processing functions. Synopsys' DesignWare ARC Sound IP is capable of delivering studio quality audio using Synopsys' Sonic Focus™ post-processing technology while simultaneously supporting long hours of playback time using Energy PRO active power management.

"The emerging Chinese audio markets and their associated standards, including DRA for Mobile Multimedia Broadcasting and Blu-ray Disc, are enabling the delivery of a high-quality audio experience in a growing number of applications," said John Koeter, vice president of marketing for IP and Systems at Synopsys. "As a leading provider of 32-bit processor cores with more than 700 million units shipped annually, Synopsys continues to help designers incorporate proven technology into emerging markets such as HD digital audio. Synopsys' DesignWare ARC Sound IP solution of silicon-proven audio processors, codecs and software provides designers with a comprehensive, end-to-end audio solution for a full range of audio standards."

DRA is an audio coding and decoding technology used to implement the Multi-channel Digital Audio Codec Specification, which was approved as China's electronic industry standard (SJ/T11368-2006) and National Audio Standard (GB/T 22726-2008). DRA is included in the Blu-ray Disc BD-ROM specification and was selected as the audio coding format for Chinese Multimedia Mobile Broadcasting (CMMB). The DesignWare ARC Sound audio processors and DRA decoder is the first commercial IP solution to support this standard, enabling 24-bit precision for all channels along with multichannel configuration support, including stereo and 5.1/6.1/7.1 surround. They also provide support for various sample rates from 8 kHz to 192 kHz. The DesignWare ARC Sound IP solution enables OEMs and SoC designers to implement HD audio in their designs, providing extended audio capabilities in applications supporting the unique audio requirements of the Chinese market.

Availability

The DesignWare ARC Sound DRA decoder, optimized for the AS211SFX and AS221BD audio processors, is available for early access customers now and is planned to be generally available in July 2011. The AS211SFX and AS221BD processors are available now. For more information, visit: https://www.synopsys.com/designware-ip/processor-solutions/arc-processors/arc-audio/arc-audio-codecs.html .

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and Verification IP for widely used protocols,analog IP, embedded memories, logic libraries, embedded test & repair IP and configurable processor cores. In addition, Synopsys offers SystemC™ transaction-level models to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, reuse tools, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits of and dates of availability of specific DesignWare ARC Sound DRA solutions. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks detailed in Synopsys' filings with the U.S. Securities and Exchange Commission, including those described in the "Risk Factors" section of the latest Quarterly Report on Form 10-Q for the fiscal quarter ended January 31, 2011.

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