Synopsys' DesignWare SuperSpeed USB 3.0 xHCI Host Controller IP Receives USB-IF Certification

Silicon-Proven DesignWare IP Lowers Design Risk and Allows Interoperability with USB 3.0-Enabled Products

MOUNTAIN VIEW, Calif., May 5, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that its DesignWare® SuperSpeed USB 3.0 xHCI (Extensible Host Controller Interface) IP has successfully passed the USB Implementers Forum (USB-IF) SuperSpeed USB certification. The xHCI specification provides a standardized method for SuperSpeed USB (USB 3.0) host controllers to communicate with the USB 3.0 software stack. To achieve certification, the IP must support the new U1 and U2 power modes as well as all four USB transfer speeds, including SuperSpeed (5.0 Gbps), Hi-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed USB (1.5 Mbps). Synopsys is the only USB IP provider with both certified SuperSpeed USB 3.0 Host and Device IP. The complete DesignWare SuperSpeed USB 3.0 IP solution offers a unified architecture, enabling designers to significantly lower integration risk by eliminating the requirement to manage two distinct USB 2.0 and USB 3.0 datapaths in their system-on-chip (SoC) designs. Optimized for small area and low-power, the DesignWare SuperSpeed USB 3.0 Host Controller is already in products that are in mass production. It is ideal for battery-powered, portable devices.

"Passing SuperSpeed USB certification is a crucial product milestone demonstrating that the Synopsys DesignWare IP meets the standards required for interoperability, which is a cornerstone for the mass adoption of USB," said Jeff Ravencraft, USB-IF president and COO. "Synopsys' proper implementation of the U1 and U2 power saving modes will help extend the battery life in future USB products."

"As a leading developer of USB 3.0 software, it was critical that MCCI partner with Synopsys, a trusted IP provider, for the development of the MCCI USB 3.0 xHCI Datapump Host Stack," said Terry Moore, CEO of MCCI. "Our close collaboration with Synopsys throughout the years has enabled us to create an interoperable USB 3.0 software platform that delivers fast SuperSpeed USB transfer speeds and full legacy support, while taking advantage of power savings from U1 and U2 modes. Whether in an embedded system, on Linux, or as a Windows driver, the MCCI software stack, combined with emulated FPGA hardware, allows developers to focus on system issues early in the development cycle."

"For the past 15 years, Synopsys has delivered high-quality USB IP solutions that have been integrated in more than 2000 designs," said John Koeter, vice president of marketing for IP and Systems at Synopsys. "The DesignWare SuperSpeed 3.0 IP is a complete, market proven and certified solution consisting of DesignWare digital controllers, PHYs and verification IP. Combined with Synopsys' virtual prototyping and HAPS® FPGA-based prototyping solutions, Synopsys' certified USB IP products help designers lower integration risk and ensure interoperability with billions of USB-enabled devices."

Availability

The silicon-proven DesignWare SuperSpeed 3.0 USB Device, Host and Dual-Role Device Controllers are available now along with, verification IP, virtual prototype and drivers. The DesignWare SuperSpeed USB 3.0 PHY IP is available in leading 65-nanometer (nm) and 130-nm process technologies now, with support for 28-nm and 40-nm process technologies scheduled to be available in the first half of 2011. For more information on DesignWare USB IP, please visit: http://www.synopsys.com/usb or follow our blog at http://www.synopsysoc.org/usb-blog.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and Verification IP for widely used protocols,analog IP, embedded memories, logic libraries and configurable processor cores. In addition, Synopsys offersSystemC™ transaction-level models to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, reuse tools, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter athttp://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys

customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the dates of availability of specific DesignWare SuperSpeed USB 3.0 PHY IP solutions for 28-nm and 40-nm process technologies. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks detailed in Synopsys' filings with the U.S. Securities and Exchange Commission, including those described in the "Risk Factors" section of the latest Quarterly Report on Form 10-Q for the fiscal quarter ended January 31, 2011.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Stephen Brennan
MCA
650-968-8900 x114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.