# Synopsys Design Compiler Graphical Cuts Design Time at Exar

Exar Engineers Detected and Fixed Routing Congestion Hot Spots in Synthesis Before Hand-off to Physical Implementation

MOUNTAIN VIEW, Calif., April 19, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Exar Corporation, a provider of software and subsystem solutions for industrial, datacom and storage applications, has broadly deployed Synopsys' Design Compiler® Graphical RTL Synthesis solution, a key component of the Galaxy™ Implementation Platform, to shorten its IC design schedule. Previously, engineers at Exar performed multiple time-consuming iterations between synthesis and place and route due to routing congestion issues identified late in the design flow by the backend design teams. Using Design Compiler Graphical, on their latest networking IC, Exar engineers detected and fixed routing congestion hot spots early during synthesis before passing the design on for physical implementation. This allowed them to shorten their design schedule by three weeks. Consequently, Exar has made Design Compiler Graphical an integral part of its design flow in order to shorten design time across all ICs.

"Using Design Compiler Graphical's congestion analysis and optimization capabilities on our latest networking chip, we were able to address routing congestion issues during synthesis prior to place and route, enabling the design to be accomplished much faster," said Scott Peterson, division vice president of engineering design services at Exar Corporation. "With Design Compiler Graphical, a design block that would require significant effort to route was taken out of the critical path."

Design Compiler Graphical extends Synopsys' DC Ultra™ topographical technology to predict routing congestion hot spots early in the design flow, providing designers with visualization of congested circuit regions and allowing them to perform specialized synthesis optimizations to minimize congestion in these areas. Additionally, it provides access to the design planning capabilities of Synopsys' IC Compiler from within the synthesis environment, giving RTL designers the ability to explore and converge on an optimal floorplan faster. It also produces physical guidance to IC Compiler physical implementation, tightening timing and area correlation up to 5 percent while speeding IC Compiler placement by 1.5X. By enabling RTL designers to efficiently achieve an optimal floorplan and passing physical guidance to IC Compiler, Design Compiler Graphical doubles the productivity of the entire synthesis and place-and-route flow.

"Customers such as Exar are rapidly adopting Synopsys' Design Compiler Graphical to shorten their design schedule and stay competitive," said Bijan Kiani, vice president of product marketing, design and manufacturing products, at Synopsys. "By providing early visibility into design issues such as routing congestion, Design Compiler Graphical helps accelerate design implementation, deliver more predictable schedules and lower overall project costs."

**About Synopsys**

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.



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