

Synopsys Unveils DC Explorer for Early RTL Exploration

Solution Accelerates Design Implementation through Early Exploration While Tolerating Incomplete Data

MOUNTAIN VIEW, Calif., March 28, 2011 [PRNewswire/](#) -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today introduced DC Explorer, the latest addition to the Galaxy™ Implementation platform, to significantly speed up development of high-quality design data. To meet aggressive schedules for today's massively integrated, multimillion-instance, "Gigascale" designs, engineers need an RTL exploration solution that enables them to quickly and efficiently perform what/if analyses of various design configurations – even before the design data is complete – and create a better starting point for the implementation flow. DC Explorer addresses this challenge by delivering 5X faster runtime and 10 percent timing and area correlation to DC Ultra™ RTL Synthesis. It also tolerates incomplete design data and therefore can be used very early in the design flow to guide the development of high-quality RTL and constraints, enabling a highly convergent design flow. These new productivity benefits DC Explorer delivers will be highlighted today by users at the Synopsys Users Group (SNUG™) meeting in San Jose, Calif.

"Improving productivity at the early stages of design development can significantly accelerate our IC implementation flow," said Giancarlo Sada, deputy manager of the Digital Solutions and Pilot Projects team of Central CAD and Design Solutions organization at STMicroelectronics. "We ran DC Explorer on multiple designs at various stages of development and have seen at least 4X faster runtime and 10 percent correlation to DC Ultra. This will enable our designers to efficiently assess various implementation alternatives early in the flow, tune the design data and create a highly convergent and faster design flow."

At the early RTL design development stages of today's large and complex ICs, the design data comes from multiple sources at varying levels of consistency and completeness. Engineers lack a fast and efficient way to explore and improve the data, fix design issues and create a better starting point for RTL synthesis that will lead to a highly convergent implementation flow. DC Explorer provides designers with the RTL exploration capabilities they need, helping them to efficiently identify potential design improvements and issues prior to implementation. In addition, when the input RTL, constraints and library models available are incomplete, DC Explorer generates comprehensive reports on what needs to be completed and fixed, speeding up the process of design creation. Lastly, script compatibility with Design Compiler® RTL Synthesis makes DC Explorer very easy to use and deploy into existing customer flows.

"Synopsys is continuously focused on helping our customers improve their productivity and shorten design cycles for their Gigascale system-on-chip devices," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "DC Explorer delivers the next significant productivity boost to IC designers, enabling them to perform RTL exploration very early in the design flow, improve the quality of their design data and significantly accelerate schedules."

Availability

DC Explorer is currently in limited customer availability.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <http://www.synopsys.com/>.

Synopsys, Galaxy, Design Compiler and DC Ultra are registered trademarks or trademarks of Synopsys, Inc. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.

650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE Synopsys, Inc.
