Synopsys Introduces Proteus LRC for Lithography Verification

Provides Lowest Cost of Ownership and High Accuracy for 28nm and Below

SAN JOSE, Calif., March 1, 2011 /PRNewswire/ -- **SPIE Advanced Lithography**—Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today introduced Proteus LRC for lithography verification. Proteus LRC provides comprehensive, process-window-aware checking features to identify locations in a design that are sensitive to process variations, thereby enabling corrective action to be taken prior to committing a design to manufacture. Proteus LRC is integrated into the Proteus Mask Synthesis flow and is targeted for use by OPC and mask data preparation groups at semiconductor manufacturers like Micron Technology, Inc.

Proteus LRC is designed to deliver the accuracy needed for 28-nanometer (nm) and below technology by using industry-proven optical proximity correction (OPC) models and rigorous first-principle models from embedded Sentaurus Lithography technology. It is imperative for lithography rule check (LRC) tools to accurately predict and verify the critical dimension (CD) variation through the process window to help ensure that adequate process margins are maintained for optimum wafer yield. The Sentaurus Lithography technology embedded in Proteus LRC allows easy access to rigorous first-principle models for resist profiles and topography effects when identifying at-risk hotspots and determining the appropriate course of action.

"At Micron, it is imperative not to miss any hotspots that would have a negative impact on yield," said Anthony Krauth, R&D advanced mask development manager at Micron Technology, Inc. "Proteus LRC has robust checking algorithms and predictable models that help ensure we don't miss critical issues."

With the implementation of new manufacturing techniques like extreme ultraviolet lithography (EUV) and double-patterning technology (DPT), the verification process becomes even more challenging. Proteus LRC includes DPT-specific checking functionality that provides error detection for each exposure and mask misalignment condition with a consolidated results viewing environment. By taking advantage of Synopsys' Proteus Pipeline Technology, which was introduced at SPIE Advanced Lithography 2008, Proteus LRC is able to efficiently handle the full-chip layout requirements of EUV.

As transistor density continues to increase with each new technology node, meeting turn-around-time goals in a production flow becomes more difficult. Effectively meeting this challenge requires efficient use of hardware resources, in addition to advancements in software applications. Proteus LRC has been fully integrated in the Proteus Mask Synthesis flow with near-linear scalability to hundreds of standard x86 processor cores, allowing full control over turn-around time and delivering the lowest cost of ownership.

"We integrated Proteus LRC into the Proteus Mask Synthesis flow to allow semiconductor manufacturers to run the entire OPC flow efficiently on standard hardware resources," said Howard Ko, senior vice president and general manager of the Silicon Engineering Group at Synopsys. "We also embedded Sentaurus Lithography technology in Proteus LRC to provide OPC engineers with the ability to analyze critical hotspots with the highest level of accuracy."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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