Synopsys' DesignWare Universal DDR Memory Controller Delivers up to 30 Percent Lower Latency and Increases System Performance

Enhanced Architecture Enables Faster Access to Off-chip DRAM and Delivers Higher Throughput for SoC Designs

MOUNTAIN VIEW, Calif., Feb. 9, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the release of its enhanced DesignWare® Universal DDR Memory Controller, which delivers up to 30 percent lower latency and offers up to 15 percent higher throughput than the previous generation controller. The DDR Memory Controller offers new features such as high-priority bypass and configurable 'look-ahead.' The high-priority bypass option allows designers to improve latency by bypassing the scheduling algorithm, allowing immediate access to the DRAM. The configurable 'look-ahead' feature provides intelligent scheduling to maximize throughput by prioritizing out-of-order transactions to the DRAM, allowing designers to make trade-offs between area and performance. The Memory Controller also offers a DFI 2.1-compliant interface to the DDR PHY, delivers memory system performance of up to 2133 Mbps and supports the DDR3, DDR2, LPDDR and LPDDR2 SDRAM standards.

"As the leading supplier of SoCs for femtocells and small-cell base stations, we rely on Synopsys, a trusted IP vendor, to provide us with a high-quality DDR IP solution that further helps us differentiate our products in the market," said Will Robbins, vice-president of Silicon, Tools and Platforms at Picochip. "Synopsys' continued advancements in DDR IP allow us to reliably develop high-performance memory systems that are optimized for both throughput and latency."

"Synopsys is continually improving the performance and features of our DDR memory controller solutions," said John Koeter, vice president of marketing for IP and Systems at Synopsys. "By combining the best features of the previous-generation DesignWare Universal DDR memory controller with the best features of the Intelli™ architecture acquired from Virage Logic, we are able to significantly decrease the latency and improve throughput in this generation. With a proven track record of more than 250 DDR IP design wins amongst more than 200 customers, Synopsys offers designers a low-risk path to silicon success."

The DesignWare Universal DDR Memory Controller is part of Synopsys' comprehensive DesignWare DDR IP offering that consists of digital controllers and PHY IP supporting DDR, DDR2, DDR3, LPDDR and LPDDR2. The DesignWare DDR IP supports leading 130-nm, 90-nm, 65-nm, 55-nm, 45/40-nm and 32/28-nm technologies.

Availability

The enhanced version of the DesignWare Universal DDR Memory Controller single-port configuration is scheduled for availability in March 2011. For more information on DesignWare DDR IP, please visit: http://www.synopsys.com/IP/InterfaceIP/DDRn/Pages/default.aspx.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and Verification IP for widely used protocols,analog IP, embedded memories, logic libraries, embedded test & repair IP, audio post-processing software and configurable processor cores. In addition, Synopsys offersSystemC transaction-level models to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, reuse tools, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits and date of availability of the enhanced version of the DesignWare Universal DDR Memory Controller single-port configuration. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2010 entitled "Risk Factors."

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