

Synopsys Invites Cadence Incisive and Mentor Graphics Questa Users to the Verification FastForward Program

VCS support for OVM 2.1.1 and the upcoming UVM 1.0 enables smooth migration to faster verification

MOUNTAIN VIEW, Calif., Feb. 3, 2011 [PRNewswire/](#) -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the verification FastForward migration program. The program helps Cadence® Incisive® and Mentor Graphics® Questa® users to migrate to the VCS® functional verification solution and benefit from its superior technologies. These include: innovative performance engines; the industry's broadest SystemVerilog support for VMM, OVM, and the UVM(TM) methodologies; a powerful constraints solver; new coverage closure technologies; unique low power verification capabilities; and a rich portfolio of verification IP. With the combination of the verification FastForward program and VCS' state-of-the-art technologies, users can achieve up to 2X faster verification closure.

"Network security consistently imposes more design complexity, which necessitates a high-performance, efficient, and scalable verification solution, especially given our mounting time-to-market pressures," said Barun Kar, senior director of hardware engineering at Palo Alto Networks. "We migrated to VCS because it offered a significant performance advantage over other solutions, and it proved a good fit for our growth plans as we move to larger designs, targeted for both high-end FPGAs and ASICs."

"We migrated our verification environment to VCS in 2009," said Rich Schofield, principal verification engineer at Acme Packet, the leading provider of session border controllers. "Our Net-Net portfolio of hardware platforms utilizes custom high speed communication ICs, and we require a high performance verification environment with robust SystemVerilog support. After evaluating offerings from several vendors, we chose Synopsys VCS."

The Verification FastForward Program

The verification FastForward program includes technical services, training, and expert verification support. As part of the program, users can expect services such as assistance with OVM to UVM testbench migration, migration of scripts, verification IPs, and regression environment, as well as training for efficient deployment of VCS and UVM methodology.

The verification FastForward migration program has been in pilot since 2009, during which time numerous verification teams have migrated to VCS and have significantly improved their verification effectiveness and productivity. These teams span various market segments, company sizes, and geographies and are working on diverse design sizes, verification methodologies, and technology nodes.

VCS Support for VMM, OVM 2.1.1, and UVM 1.0

Today Synopsys also announced VCS support for the upcoming UVM 1.0 methodology. Combined with existing support for VMM and OVM 2.1.1, this offers VCS users the industry's most broad and mature SystemVerilog support.

"AMD has used Synopsys VCS with OVM since 2008," said Warren Stapleton, senior fellow at AMD. "The VCS SystemVerilog implementation is mature and we are happy with our decision to use the OVM framework with VCS, as we have seen improved productivity and user advantages. We look forward to moving to UVM to achieve the same advantages, along with the strength of it being an Accellera standard."

"We applaud Accellera's UVM effort," said Manoj Gandhi, senior vice president and general manager of the Verification Group at Synopsys. "This effort acknowledges the industry's further alignment around SystemVerilog. As verification challenges grow, we continue our focus and investment in leading SystemVerilog technologies to enable the next levels of innovation in performance, debug, coverage closure, and verification IP."

About VCS

According to advanced designs data collected by Synopsys, 90 percent of designs at 32nm (and more advanced nodes) and 60 percent of designs at 45nm are verified with VCS. Used by a majority of the world's top 20 semiconductor companies as their primary verification solution, VCS includes high-performance simulation engines, constraint solver engines, native testbench, broad SystemVerilog support, verification planning, coverage analysis and closure, and integrated debug environment.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics

market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <https://www.synopsys.com/>.

Synopsys and VCS are registered trademarks of Synopsys, Inc. Cadence and Incisive are either trademarks or registered trademarks of Cadence Design Systems, Inc. in the United States and/or other jurisdictions. Mentor Graphics and Questa are registered trademarks of Mentor Graphics Corp. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contact:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Andrea Zils
MCA, Inc.
650-968-8900 x135
azils@mcapr.com

SOURCE Synopsys, Inc.
