Synopsys Collaborates with Industry Consortium on Solutions to Model Latest 28-nm Parasitic Effects

IMTAB Group in IEEE-ISTO Ratifies Interconnect Technology Format Extensions

MOUNTAIN VIEW, Calif., Feb. 1, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced new extensions to its open source-licensed Interconnect Technology Format (ITF) which enables modeling of more complex device structures and interconnect layers for parasitic extraction tools at 28-nanometer (nm) and below process technologies. Synopsys collaborated with the members of the Interconnect Modeling Technical Advisory Board (IMTAB) of the IEEE Industry Standards and Technology Organization (IEEE-ISTO) to define these new extensions, which have been ratified by IMTAB members including Altera Corporation, AMD, Apache Design Solutions, GLOBALFOUNDRIES, LSI Corporation, Magma Design Automation, NVIDIA, Qualcomm, STMicroelectronics and Synopsys.

"IMTAB members are dedicated to addressing the industry's most complex parasitic modeling challenges seen in advanced silicon processes and are providing an efficient technical forum to facilitate the evolution of an interoperable format for interconnect modeling," said Bari Biswas, chair of IMTAB and senior director of engineering for extraction solutions at Synopsys. "It is encouraging to see ITF licensed by more than 25 semiconductor companies and the top 4 EDA vendors since its open source availability in June of 2010. We look forward to building on the momentum and broad adoption of ITF as the interoperable format of choice for advanced node design."

The new IMTAB ratified extensions to ITF include:

- Device conductor layer type specification to define a conductor's function based on the geometric characteristics
- High-k gate oxide thickness and dielectric constant specification for accurate capacitance calculation
- 2-dimensional table to model rectangular via etch as a function of length and width
- Area-dependent temperature coefficient table for accurate via resistance calculation
- Model format to describe through-silicon via (TSV) for on-chip extraction to support 3-dimensional IC and silicon interposer design methodologies

"IMTAB members are collaborating to address real-world challenges facing the semiconductor industry in sub-28-nanometer process nodes," said Peter Lefkin, business development and marketing executive at IEEE-ISTO. "The fast pace of innovation in the ITF modeling, as driven by IMTAB, will help the industry coalesce around a single proven format to improve tool interoperability and speed design flows, offering tremendous benefits to all."

The next IMTAB meeting will be held on Wednesday, March 23, 2011. The agenda, focusing on 20nm modeling, will be posted on the IEEE-ISTO's IMTAB website: www.imtab.org.

Requests for ITF format enhancements come from the IMTAB membership as well as from the overall interconnect modeling format user community. Companies interested in membership in IMTAB may contact IEEE-ISTO at imtab@ieee-isto.org.

About ITF

Synopsys' Interconnect Technology Format (ITF) provides detailed modeling of interconnect parasitic effects that enables designers to perform accurate parasitic extraction for timing, signal integrity, power and reliability signoff analysis. ITF offers a flexible and innovative format to accurately model the effects of increased process variation at advanced process technologies. ITF has been evolving for more than 10 years and is the semiconductor industry's most widely used interconnect modeling format; proven on thousands of production designs. It is supported by leading semiconductor foundries, integrated device manufacturers, and EDA tool providers.

The ITF format can be licensed for no charge through Synopsys' Technology Access Program (TAP-in™). The latest specifications for ITF can be found at: https://www.synopsys.com/Community/Interoperability/Pages/TapinITF.aspx

About IEEE-ISTO

IEEE-ISTO is the premier trusted partner of the global technology community for the development, adoption, and certification of industry standards. Its mission is to facilitate the life-cycle of industry standards development through a dedicated staff

committed to offering vendor neutrality, quality support and member satisfaction. Fostering the market acceptance, adoption and implementation of standardized technologies, IEEE-ISTO Programs span the spectrum of today's information and communications technologies. To find out more about IEEE-ISTO, visit www.ieee-isto.org.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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