

Media Advisory/Alert: Synopsys to Showcase DesignWare IP, FPGA Design, FPGA-Based Prototyping and HSPICE Solutions at DesignCon 2011

SANTA CLARA, Calif., Jan. 28, 2011 [PRNewswire/](#) -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, will showcase its latest DesignWare® DDR PHY Compiler, Synplify® FPGA design tools, HAPS® FPGA-based prototyping platform, and HSPICE® solutions at DesignCon 2011 in Santa Clara, California on February 1-2, 2011. See live demonstrations, speak with our product experts and find out how Synopsys can help you achieve predictable success.

DesignCon® is the definitive event for electronic design experts spanning chip, package, board, and system domains, addressing common issues in signal integrity, power management, interconnection and design verification.

To find out more about Synopsys participation at DesignCon, visit our website at <https://www.synopsys.com/IP/Pages/DesignCon2011.aspx>

WHAT: Synopsys will be showcasing its latest developments in DesignWare DDR IP, FPGA Design, FPGA-based prototyping, AMS/custom design and HSPICE solutions in Synopsys Booth #606. In addition, Synopsys will be participating in a number of presentations, tutorials and panels at the show.

Synopsys will also host its first HSPICE Special Interest Group (SIG) event on the evening of January 31, 2011 at the Santa Clara Hyatt hotel, coincident with DesignCon. Attendees will have an opportunity to hear what industry leaders have to say about using HSPICE in some of today's most challenging designs and talk with Synopsys HSPICE R&D personnel as well as HSPICE Integrator Program (HIP) partners. Those interested in attending can register online.

WHEN: February 1-2, 2011

WHERE: Santa Clara Convention, 5001 Great America Pkwy., Santa Clara, CA 95054, Synopsys booth #606

EXHIBIT HOURS:

Tuesday, February 1 12:30pm - 6:00pm

Wednesday, February 2 12:30pm - 6:00pm

Visit booth #606 to enter a drawing for Bose headphones

DEMO DESCRIPTIONS:

- **DesignWare DDR PHY Compiler**

Synopsys' DesignWare DDR PHY Compiler demonstration will show how to optimize a DDR PHY for pinout, area and performance. In addition, we will highlight several features of the DesignWare DDR3/2 PHY IP in 40nm technology as it achieves speeds up to 1600Mbps utilizing Synopsys' characterization platform.

- **DesignWare HDMI 1.4 Tx and RX IP**

HDMI is gaining significant traction in delivering 3D functionality in digital home theater systems, gaming consoles and other portable multimedia devices. The Synopsys DesignWare HDMI 1.4 IP supports the latest HDMI 1.4a specification, including various 3D formats. This demonstration will show how Synopsys' silicon-proven HDMI 1.4 IP will deliver 3D content to a high resolution display.

- **Synplify FPGA Design Tools**

In this demonstration we will address key challenges faced by today's FPGA designers such as fast timing closure for demanding applications, timing-driven synthesis for cost reduction and incremental design flows. New hierarchical design capability for supporting distributed development, IP integration and reuse will be highlighted along with new technology for dynamic power reduction.

- **HAPS FPGA-Based Prototyping Solution**

Synopsys' FPGA-based prototyping solutions enable pre-silicon software development and hardware/software co-verification of complete systems at near real-time operating speeds using real-world interfaces. We will demonstrate the new UMRBus for the HAPS-60 series which delivers programmability and flexibility without compromising "at-speed" system performance.

- **HSPICE Precision Parallel Technology**

With up to 7X speed up on eight cores, 10-million-element capacity, comprehensive analysis and out-of-the-box convergence, analog design teams can use HSPICE Precision Parallel technology to accelerate verification of circuits across process corners and minimize the risk of missing project timelines and silicon respins. See how HSPICE can improve analog designers' productivity through superior performance and accuracy and tight integration with Galaxy Custom Designer®.

- **HSPICE Statistical Eye Diagram Analysis**

Analysis of high-speed serial interfaces requires processing of millions of bits of data. Using traditional transient analysis to evaluate eye diagrams and bit error rates (BER) leads to impractically long simulation times. Synopsys will show how the HSPICE statistical eye diagram feature can evaluate eye diagrams and bit error rate quickly and accurately. We will also demonstrate statistical setup, input syntax and outputs.

Synopsys Papers, Presentations and Tutorials at DesignCon

- Tutorial: Verification Planning and Management in a System-Level Design Flow
- Panel: Challenges in Designing, Verifying, and Integrating Power-managed IPs
- Panel: Phase Noise and Jitter Translations for Signal Integrity
- Paper: Life Without Termination - Delivering Successful LPDDR/LPDDR2 Interfaces
- Presentation: PDKs for Analog IC Design - A Stakeholder Discussion
- Presentation: Cloud Computing for Electronic Co-Design: Challenges and Opportunities

For more information on the products being showcased at DesignCon, please visit the following:

- DesignWare IP - <https://www.synopsys.com/designware>
- FPGA Design - <https://www.synopsys.com/fpga>
- FPGA-based prototyping solutions - <https://www.synopsys.com/fpga-based-prototyping>
- HSPICE- <http://www.hspice.com/>
- Synopsys' unified custom design solution - https://www.synopsys.com/custom_design.aspx

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <https://www.synopsys.com/>.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.

650-584-8635

sgulizia@synopsys.com

Stephen Brennan

MCA, Inc.

650-968-8900, ext.114

sbrennan@mcapr.com

Synopsys, DesignWare , HAPS, HSPIICE and Synplify are registered trademarks of Synopsys, Inc. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

SOURCE Synopsys, Inc.
