Synopsys' IC Validator Completes Qualification for TSMC's 40-nm and 65-nm iDRC/iLVS Physical Verification

Runset Availability Enables Faster Tapeouts with In-Design Physical Verification

MOUNTAIN VIEW, Calif., Nov. 17, 2010 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that its IC Validator physical verification product is qualified for TSMC's 40-nm and 65-nm interoperable DRC/LVS runsets, and is immediately available to TSMC customers. IC Validator, part of the Galaxy™ Implementation Platform, is an ideal add-on to IC Compiler for In-Design physical verification. By enabling physical verification within the implementation flow, IC Validator enables place and route engineers to accelerate time to tapeout and improve manufacturability. TSMC's qualification of IC Validator brings the unique advantages of the In-Design flow to the broad range of design teams utilizing TSMC's 40-nm and 65-nm process technologies.

"The iDRC and iLVS format, a key component of TSMC's Open Innovation Platform™ initiative, allow us to streamline design rule development and deployment, ensuring consistent interpretation across EDA partners and timely availability for our customers," said Suk Lee, director of design infrastructure marketing at TSMC. "Having successfully completed our rigorous qualification process, Synopsys' IC Validator is now a qualified solution for our 40-nanometer and 65-nanometer process technologies with immediate iDRC/iLVS runset availability for our common customers."

IC Validator boosts performance by parsing interoperable rule decks into efficient atomic instructions suitable for highly parallel execution. Furthermore, IC Validator leverages its scalable hybrid data and command-processing engine to offer a powerful platform for coding and validating the complex polygon and edge-based rules required for emerging process nodes. IC Validator is production-ready and has been successfully used for tape-outs at leading fabless design companies, semiconductor manufacturers and foundries.

IC Validator and IC Compiler share data models and processing engines, resulting in an integrated In-Design physical verification flow designed to deliver signoff-level accuracy coupled with superior productivity. Compared to the traditional "implement-then-verify" approaches, the In-Design flow avoids late-stage surprises and mitigates costly iterations between place-and-route and signoff. In-Design physical verification provides functionality such as incremental DRC, automatic error detection and correction, optimal metal-fill insertion and rapid ECO validation, all within the place-and-route environment, enabling physical design engineers to generate manufacturing-clean designs that should pass the final signoff check without difficulty, speeding overall time to tapeout.

"Synopsys supports standardization and interoperability, which enables our customers to achieve higher efficiency," said Antun Domic, senior vice president and general manager, implementation group at Synopsys. "We closely collaborated with TSMC to develop the interoperable file format and qualify IC Validator for TSMC's advanced process technologies. This qualification enables us to bring the proven advantages of In-Design physical verification to a rapidly growing number of design teams working at 65 nanometers and below."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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