Synopsys Expands Synthesis-Based Test Technology to Increase Designer Productivity

Unveils Plan to Accelerate Implementation of Higher Quality, Lower Cost Test

MOUNTAIN VIEW, Calif., Nov. 1, 2010 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced plans to expand test technology embedded in Synopsys' RTL synthesis to address the need for higher defect coverage, lower test cost and faster yield analysis while simultaneously minimizing the impact on design goals and project schedules. Design teams currently using Synopsys' RTL synthesis and test solution are able to quickly implement compression to lower digital logic test costs, handle pin-limited test methodologies and execute on-chip testing of high-speed blocks like USB and PCI Express® cores. Commencing today and continuing over the next twelve months, Synopsys is rolling out expanded synthesis-based test technology to provide defect coverage of embedded memories, lower test cost significantly with higher compression for pin-limited test and extremely large designs, and enable designers to rapidly analyze defective silicon devices. As with Synopsys' widely-deployed DFTMAX™ compression, the new test technology will enable designers to achieve optimal quality-of-results and eliminate time-consuming iterations between design and test.

"Our ongoing collaboration with Synopsys has produced several widely adopted, leading-edge test technologies such as managing power of the device on the tester and high defect coverage using a limited number of pins," said Roberto Mattiuzzo, Design For Excellence manager in Technology R&D - Central CAD and Design Solutions at STMicroelectronics. "We continue to work together on more technology embedded in synthesis to further increase our test quality, control test costs and allow us to quickly analyze defective silicon under very tight schedules."

"Synopsys delivers test technology that keeps pace with our evolving requirements," said Bruce Fishbein, director of engineering at Cavium Networks. "As our designs become larger and more complex, test technology based on synthesis for defect coverage of digital logic will allow our designers to be more productive and continue to deliver high quality silicon on time."

Testing complex chips requires embedding dedicated test logic throughout the entire design. Implementing this test logic outside the synthesis flow adversely impacts design characteristics such as performance and power consumption, leading to iterations between synthesis and test that lengthen project schedules. In contrast, Synopsys' solution implements test within RTL synthesis to minimize the impact on design power, timing and area, accelerating convergence on both design and test goals. Synopsys is expanding this synthesis-based test technology to further increase designer productivity, improve quality and lower cost across all areas of manufacturing test and yield analysis, including the following:

Memory Test and Repair – In widespread use today, the DesignWare™ STAR Memory System delivers high-coverage test and repair of embedded memories. Synopsys plans tighter integration with synthesis-based test to ensure fast turnaround time and maximum scalability.

Higher Compression – To accommodate the need for even lower test cost for pin-limited methodologies as well as extremely large designs, Synopsys will provide higher compression utilizing synthesis-based technology to maximize designer productivity.

Faster Yield Analysis – New integration between TetraMAX® ATPG and Yield Explorer yield analysis will enable designers to rapidly debug defective parts from a relatively small number of wafers.

"Our customers constantly need to shorten their schedules and improve throughput for all aspects of design and test," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "To address this need, we are expanding our synthesis-based test technology to further increase the productivity gains, test quality and test cost savings designers achieve with Synopsys' solution."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe,

Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits and availability of Synopsys' expanded synthesis-based test technology. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2009, and subsequent forms 10-Q, entitled "Risk Factors."

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE Synopsys, Inc.