Synopsys Power-Aware Test Speeds Time to Volume Production at Realtek

Reducing Power Consumption and IR Drop During Manufacturing Test Enables Faster Delivery of Working Silicon

MOUNTAIN VIEW, Calif., Oct. 26 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Realtek Semiconductor Corporation, one of the world's leading network and multimedia IC providers, deployed Synopsys power-aware test to avoid power issues during test and accelerate production testing of its new digital media processor. Excessive power consumption during manufacturing test leads to overheating, IR drop, and other effects that can cause devices to fail, impacting profitability and delaying production ramp. Designers at Realtek avoided these issues by reducing the device power consumption at test time using advanced power-aware capabilities in Synopsys' DFTMAX™ compression and TetraMAX® ATPG tools, integral components of the Galaxy™ Implementation Platform. As a result, Realtek delivered high-quality parts in volume quantities weeks earlier and at lower cost than previously possible.

"Our product teams can ramp-up to volume testing faster with Synopsys power-aware test because we spend less time debugging power-related issues," said Realtek's vice president and spokesman, Jessy Chen. "An added benefit is that we can test our products across a much wider range of operating environments, including lower supply voltage conditions."

Synopsys power-aware test employs a variety of synthesis-based design-for-test (DFT) and automatic test pattern generation (ATPG) techniques that reduce power consumption during test while minimizing the impact test logic has on design timing, area, power and congestion. This approach eliminates time-consuming iterations between RTL synthesis, test and physical implementation, helping designers converge on both test and design goals faster. DFTMAX compression and TetraMAX ATPG work in tandem to keep the device power during test at the same level as normal system operation, preventing false rejections due to IR drop. By also substantially reducing average power to circumvent over-heating, the test program can execute faster, thereby reducing total test time and cost.

"Fully-functional silicon can be erroneously rejected at test time due to power issues associated with the testing process itself," said Bijan Kiani, vice president of product marketing at Synopsys. "Customers such as Realtek are addressing these issues in the design phase by using Synopsys power-aware test to maintain high gross margins and avoid costly production delays while meeting their defect coverage and cost goals."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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