Media Advisory/Alert: Expert Static Timing Users Share Results About Latest Synopsys Timing Innovation -- PrimeTime HyperScale Technology

MOUNTAIN VIEW, Calif., Oct. 21 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, will host a PrimeTime® Special Interest Group (SIG) event in Silicon Valley unveiling the latest user results with Synopsys' PrimeTime HyperScale Technology, the next-generation static timing analysis (STA) solution for large-chip hierarchical design. Speakers include timing experts from AMD, NVIDIA and others.

To register to attend this event, or for additional information, please visit: https://www.synopsys.com/cgi-bin/ptsig10/reg1.cgi

TOPIC TO BE COVERED: PrimeTime HyperScale Technology – Extending Static Timing Analysis Beyond 500 Million Instances

WHAT: PrimeTime SIG 2010 Luncheon

WHEN: October 27, 2010

WHERE: Synopsys Sunnyvale office, Building 2, 455 North Mary Avenue, Sunnyvale, CA 94085

EVENT HOURS: 12:00 pm – 2:00 pm

DESCRIPTION: Static timing users are benefiting from the runtime boost offered by multicore-enabled software like PrimeTime. However, as more design teams are developing SoCs in the range of 50 to 100 million instances, achieving overnight turnaround for full-chip STA requires new thinking and new static timing innovation. In June 2010, Synopsys announced PrimeTime HyperScale technology, delivering the next 5-10X boost in performance and capacity for large full-chip STA.

Attendees will get first-hand information from early users on deploying Synopsys' PrimeTime HyperScale technology and how it works in concert with the hierarchical physical implementation methodology used to design large SoCs to deliver a significant productivity boost. The presentation by Synopsys R&D will provide insight on two key PrimeTime HyperScale technology innovations: 1) reuse of block-level timing information without the limitations of previous generations of timing models; and 2) auto updating of block and chip timing context for faster timing convergence.

For more information on Synopsys' PrimeTime HyperScale Technology, please visit:
https://www.synopsys.com/Tools/Implementation/SignOff/PrimeTime/Pages/HyperScale-Tech.aspx

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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