100 Tapeouts Underscore Rapid and Broad Acceptance of Synopsys' In-Design Physical Verification

Top Semiconductor Manufacturers Standardize on In-Design Physical Verification with Synopsys IC Compiler and IC Validator

MOUNTAIN VIEW, Calif., Oct. 12 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that its award-winning Galaxy™ Implementation Platform product, IC Validator, for In-Design physical verification within IC Compiler, has been successfully used for more than 100 tapeouts at advanced process nodes. Coming so soon after IC Validator's 2009 launch, this milestone is a strong indicator of the requirement for a different physical verification use model. In contrast to the traditional stand-alone physical verification approach performed at the end of the design cycle, the new In-Design approach is designed to enable foundry-accurate checking as an integral part of place-and-route, thereby avoiding late-stage surprises and accelerating time-to-tapeout. Leading semiconductor companies including Renesas Electronics Corporation, Samsung, Toshiba Corporation and several others, are actively standardizing on In-Design physical verification using Synopsys' IC Validator.

"In-Design physical verification is a simple concept, yet it represents a marked departure from the usual approach of post-design physical verification and offers huge improvements in design productivity," said Hideki Yamada, Group Manager, Design Methodology Development Group, Toshiba Corporation Semiconductor Company. "As manufacturing requirements and time-to-market pressures continue to stress our tapeout schedules, In-Design physical verification has proven to offer a critically needed reduction in total turnaround time. Given the observed benefits, we have standardized on In-Design physical verification with IC Validator for our 65 nanometer and below designs."

As feature geometries shrink, the number and complexity of design rule checks (DRC) required to achieve manufacturing compliance grows exponentially. This has severely strained traditional physical verification flows, which are predominantly post-processing oriented and rely on modifications to the design after GDSII has been generated. These flows can induce multiple discover-then-fix iterations and can lead to suboptimal results. Metal-fill insertion, a mandatory manufacturability step at the advanced nodes, exemplifies this issue. Physical designers stream out the timing-closed, post-fill design for signoff validation and then stream it back in to fix any signoff errors flagged during physical verification. This time-intensive, iterative process is typically repeated on each block until the post-fill design is both signoff qualified and timing clean. The same concerns apply to more generalized design-rule checking. As the number and complexity of rules increase, the current post-processing approach can lead to several late-stage surprises that not only increase the frequency of these expensive iterations but can significantly impact tapeout schedules.

With In-Design physical verification, IC Validator and IC Compiler address the manufacturability issues within the place-and-route environment. The seamless integration enables an optimal metal-fill flow that is timing aware, signoff quality and void of expensive stream-outs and stream-ins. For design-rule checking, the flow utilizes foundry-endorsed signoff-quality checks, flags errors in the layout and drives automatic fixing, potentially saving days compared to the traditional approach of post-design discovery and manual fixes.

"In-Design physical verification is another example of Synopsys leading the innovation to bring enhanced productivity to the IC design community," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Crossing the 100-tapeout mark within a relatively short time speaks to the strength of the In-Design concept and its successful implementation in IC Compiler and IC Validator."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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