

Synopsys Reduces IP Integration Risk With Extensive SATA-IO Interoperability Testing

Compliance Testing Validates Quality of the DesignWare SATA IP Across Multiple Process Technologies

MOUNTAIN VIEW, Calif., Sept. 14 [PRNewswire](#)/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Synopsys' [DesignWare® Serial Advanced Technology Attachment \(SATA\)](#) IP solution has successfully passed the SATA International Organization ([SATA-IO](#)) electrical, digital and system interoperability testing for 130- to 40-nanometer (nm) process technologies. The SATA-IO interoperability testing validates Synopsys' internal testing of the DesignWare SATA IP, which includes extensive digital and mixed-signal simulation validation, hardware FPGA-based prototyping using Synopsys' HAPS® solution, and PHY test chip silicon characterization. A listing of all DesignWare SATA IP products to have passed SATA-IO interoperability testing can be found on the [SATA-IO Interoperability Building Block list website](#). Synopsys will be showcasing the DesignWare SATA IP Solution at the upcoming Intel Developer's Forum in San Francisco, booth #313, from September 13-15.

SATA-IO defines interoperability testing as the gold standard of compliance for the SATA specification. To be awarded SATA-IO interoperability, the IP must pass more than 200 tests that span electrical, digital and system interoperability. The stringent electrical tests stress the transmitter, receiver and signal integrity characteristics to verify precise signal voltage levels and jitter budget. The tests utilize some of the most sophisticated and complex test equipment available. To maintain an exemplary level of interoperability, the digital protocol tests are designed to ensure proper protocol communication across a wide range of devices. The IP is run against five separate systems that have been handpicked by the SATA-IO as representative of gold standard devices.

Synopsys offers designers a complete, silicon-proven and fully interoperable SATA IP solution consisting of the device, host, PHY and verification IP. The DesignWare SATA Host Controller includes a native high performance AMBA® 3 AXI® subsystem interface which supports eight SATA 6-Gb/s ports per controller. The DesignWare SATA Device Controller utilizes a hybrid hardware/software programming model optimized for SSD applications enabling high operational performance with minimum processor overhead. Complementing the Host and Device Controllers is the robust, low power DesignWare SATA PHY, which includes unique built-in diagnostics allowing on-chip visibility into the link performance and ATE test vectors for at-speed production testing.

"Based on Allion's experience and expertise with other compliance and interoperability programs, the SATA interoperability testing process is by far the most complete in its coverage of the specification and the hardest to pass," said James Ou, director of engineering at Allion. "The Synopsys SATA IP products excelled in compliance to the SATA specification with high margin in all electrical tests and displayed strict adherence to the digital protocol requirements. The ease to which the DesignWare SATA IP passed the interoperability testing reflects Synopsys' deep understanding of the SATA specification and its strict requirements."

"Next-generation SSD's are driving significant advancements into the storage market such as higher bandwidth, enhanced power efficiency and increased reliability," said John Koeter, vice president of the Solutions Group at Synopsys. "Synopsys' high-quality, silicon-proven IP solutions help designers quickly implement the latest SATA functionality and meet their design requirements with less risk and improved time-to-market."

Availability

The DesignWare SATA IP complete solution, consisting of the digital controller, PHY and verification IP is available now. For more information please visit: <https://www.synopsys.com/IP/InterfaceIP/SATA/Pages/default.aspx>.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare® IP portfolio includes complete [interface IP](#) solutions consisting of controllers, PHY and verification IP for widely used protocols, [analog IP](#), [embedded memories](#), [logic libraries](#), [configurable cores](#) and [SoC infrastructure IP](#). In addition, Synopsys offers [SystemC transaction-level models](#) to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, [reuse tools](#), extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: <https://www.synopsys.com/designware>.

Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <https://www.synopsys.com/>.

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