Synopsys DFTMAX Compression Cuts Pin-Limited Test Cost by 95 Percent at Silicon Image

Addresses Test Requirements for Mixed-Signal Designs with Tight Packaging Constraints

MOUNTAIN VIEW, Calif., Sept. 8 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Silicon Image, Inc., a leading provider of semiconductors and IP for the secure distribution, presentation and storage of high-definition content, employed DFTMAX™ compression, an integral part of the Galaxy™ Implementation Platform, to significantly lower manufacturing test cost and time. Silicon Image's mixed-signal multimedia design testing requirements included a tight form factor and a limited number of package pins. Using the new pin-limited test capability in Synopsys' DFTMAX, Silicon Image designers easily implemented test compression for the mixed-signal chip in just two days, substantially reducing test time, data and cost while achieving high test coverage.

"Because of the tight form factor of our package, only three scan input-output pairs were available for testing our design," said Narasimha Nookala, senior director IC engineering at Silicon Image. "DFTMAX compression for pin-limited test reduced test time and data by more than 95 percent while maintaining high defect coverage, making it a key component in the rigorous testing process we employ to deliver high quality products."

The demand for more functionality, smaller area and lower cost is leading to more stringent IC packaging constraints that limit the number of pins that can be allocated for test. In addition, to manage the complexity of large systems-on-chip, designers are deploying core-based methodologies that restrict access of embedded test compression logic to only a few chip-level pins. Multi-site testing, a technique that targets multiple die simultaneously to reduce test time, is also stimulating the demand for pin-limited test because each die has access to fewer tester channels.

Synopsys recently extended DFTMAX compression to enable predictable high compression for designs and methodologies that mandate as few as one pair of test data pins. Built into the Galaxy Implementation Platform to eliminate time-consuming iterations between synthesis, scan insertion and physical implementation, Synopsys' DFTMAX compression and TetraMAX® ATPG provide designers a comprehensive solution for meeting their most challenging quality and cost goals for test.

"Increased focus on packaging size and cost is driving the need to utilize fewer pins for manufacturing test," said Bijan Kiani, vice president of product marketing at Synopsys. "Silicon Image and other Synopsys customers are now benefiting from the superior quality of results attainable using DFTMAX compression to lower the cost of pin-limited testing."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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