Synopsys' Design Compiler Graphical Shortens Design Schedule at Oticon

Early Removal of Routing Congestion Essential to Meeting Time-to-Market and Area Goals for Next Generation Hearing-Aid DSP Chipset

MOUNTAIN VIEW, Calif., July 27 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Oticon taped out the digital signal processor (DSP) chipset for their next-generation hearing-aid devices ahead of schedule using Synopsys' Design Compiler™ Graphical RTL Synthesis, a key component of the Galaxy™ Implementation Platform. Engineers at Oticon, a world leader in the design, development and manufacture of hearing aids, needed to add new features to the next-generation DSP without increasing design area and while maintaining a very tight schedule. This was especially challenging due to the routing congestion caused by the added functionality, which could have led to multiple design iterations and a longer design schedule. To alleviate this congestion, Oticon's RTL designers deployed the congestion optimizations in Design Compiler Graphical during RTL synthesis, resulting in an easy-to-route netlist and predictable design closure ahead of schedule.

"We strive to deliver innovative hearing-aids to our customers, and minimizing the size and power consumption of these devices is critical to our success," said Mogens Balsby, director of Silicon Engines at Oticon. "As we enhanced the feature-set of our next-generation DSP, we saw severe routing congestion due to tight chip area requirements. By utilizing Design Compiler Graphical's congestion optimizations, we eliminated this routing congestion upfront without having to increase our chip area, and taped out successfully ahead of schedule."

Design Compiler Graphical extends DC Ultra™ topographical technology to predict routing congestion "hot spots" early in the design flow, providing designers with visualization of congested circuit regions and performing specialized synthesis optimizations to minimize congestion in these areas. This enables RTL designers to avoid wire-routing congestion problems that occur during detailed routing and eliminate costly design iterations.

Additionally, Design Compiler Graphical provides access to IC Compiler's design planning capabilities from within the synthesis environment, giving RTL designers the ability to explore and converge on an optimal floorplan faster. It also produces physical guidance to IC Compiler physical implementation, tightening timing and area correlation to 5 percent while speeding-up IC Compiler placement by 1.5X. By enabling RTL designers to achieve an optimal floorplan efficiently and passing physical guidance to IC Compiler, Design Compiler Graphical can double the productivity of the entire synthesis and place-and-route flow.

"Shorter, more predictable design schedules help our customers bring competitive products to market faster," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Synopsys continues to deliver innovative RTL synthesis technologies, such as congestion optimization, floorplan exploration and physical guidance to IC Compiler, enabling companies like Oticon to meet their challenging design and time-to-market goals."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:

Sheryl Gulizia

Synopsys, Inc.

650-584-8635

sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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