PrimeTime 2010 Scales Timing Analysis Beyond 500 Million Instances

HyperScale Technology Delivers 5 to 10X Boost in Performance and Capacity

MOUNTAIN VIEW, Calif., June 14 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today unveiled new PrimeTime® HyperScale technology that enables static timing analysis (STA) to scale beyond 500 million instances. PrimeTime HyperScale technology provides design engineers the insight required to solve many of the timing integration and closure problems they face with today's large system-on-chip (SoC) design flows while delivering a 5 to 10X boost in performance and capacity.

PrimeTime HyperScale technology fits seamlessly with today's large SoC physical implementation flows where designs are implemented in blocks and then assembled at the chip-level for final timing closure and signoff. It improves the timing closure process by providing design engineers a better mechanism to look at block-level timing in the context of the full-chip timing earlier in the design process. By directly reusing block-level timing analysis and constraints, the HyperScale technology enables a 5 to 10X boost in full-chip STA runtime and capacity without the accuracy limitations in current modeling techniques. Its auto generation capabilities provide design engineers with accurate and up-to-date timing contexts for the chip and block throughout the design process, leading to better decisions and enabling fewer iterations to reach timing closure.

"We have been working with Synopsys to address the challenge of scaling timing analysis and signoff processes as our designs approach half a billion instances," said Jim Miller, corporate vice president, Design Engineering at Advanced Micro Devices. "We see the PrimeTime HyperScale technology as a natural fit to deliver long-term scalability by better matching the physical implementation and timing analysis methodologies, allowing us to begin the timing closure process much earlier in the flow. We are excited at the prospects for PrimeTime HyperScale technology, and have high expectations for the potential runtime, capacity, and productivity benefits that may be possible from this approach."

The new PrimeTime HyperScale technology enhances the existing Galaxy™ Implementation Platform by providing more precise timing context to drive timing closure in IC Compiler. In addition, the HyperScale technology works with existing PrimeTime features like signal integrity (SI) analysis, advanced on-chip variation (AOCV) analysis, multi-scenario analysis and threaded multicore analysis, enabling design teams to further boost STA productivity and improve overall timing closure turn-around-time.

"As SoCs continue to increase exponentially in complexity, scalability of the design flow is a crucial factor in maintaining productivity," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "By adding HyperScale technology, the 2010.06 release of PrimeTime includes a significant innovation to extend STA scalability for the next five to 10 years. This release represents an important milestone in delivering higher design team productivity both today and in the future."

In related announcements today, Synopsys revealed two other productivity enhancements to its Galaxy Signoff product portfolio. New Rapid3D technology incorporated in Synopsys' StarRC™ Custom parasitic extraction solution provides up to a 20X extraction speedup for sub-45nm custom IC design and library characterization. In addition, the latest release of Liberty™ NCX provides up to a 7X boost in characterization speed while providing the most efficient composite current source (CCS) models for IC Compiler physical implementation and PrimeTime timing analysis, enabling designers to quickly achieve timing closure and improve productivity.

Availability

The PrimeTime HyperScale technology is in limited customer availability and available to select customers in the PrimeTime SI 2010.06 release.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com.

Forward looking statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits of the PrimeTime HyperScale technology. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen engineering difficulties, uncertainties attendant to any new product offering, and certain statements contained in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2009, and subsequent forms 10-Q, entitled "Risk Factors."

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