Samsung Electronics Achieves First-Pass 32nm Silicon Success Using Synopsys Galaxy Implementation Platform

MOUNTAIN VIEW, Calif., June 10 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Samsung Electronics' Foundry business (Samsung Foundry) has successfully taped out its first 32-nanometer (nm) system-on-chip (SoC) design using Synopsys' Galaxy™ Implementation Platform. Samsung Foundry selected the Galaxy Implementation Platform as one of its implementation solutions for its mobile application processor because the platform's seamless integration enabled them to meet timing while minimizing power consumption and adhering to the tighter design and manufacturing constraints imposed by a 32nm process. In addition, significant productivity benefits were achieved using In-Design Physical Verification. Staying within the cohesive design environment of the Galaxy platform saved time and enabled Samsung Foundry to tape out on schedule.

"Synopsys enabled us to successfully tape out at 32-nanometers on schedule and achieve first-pass silicon success," said Dr. KM Choi, vice president, Design Technology Team, System LSI, Samsung Electronics. "Using the Galaxy Implementation Platform allowed us to develop a scalable flow capable of fully addressing our design challenges. The effective integration of IC Compiler and IC Validator avoided many time-consuming iterations between physical implementation and verification. We have decided to deploy In-Design Physical Verification with IC Validator for all our future IC Compiler-based 32- and 45-nanometer designs."

In-Design technology provides a productivity boost over traditional flows by enabling physical verification during the physical design. The traditional approach of first implementing then verifying the design leads to many iterations between physical verification and implementation, which can result in significant schedule delays. Synopsys' integration of IC Validator within IC Compiler allowed Samsung Foundry to optimize metal fills that were timing-aware and of signoff quality. The new approach saved time by avoiding unnecessary data transfers and eliminating costly iterations while producing a clean, error-free layout.

Samsung Foundry deployed the Synopsys DC Ultra™ synthesis solution with topographical technology and the DesignWare® Library to accurately predict performance of the design during synthesis. The tight integration within the Galaxy platform reduced iterations between synthesis and layout. The IC Compiler MCMM capability was employed by Samsung Foundry to optimize across several scenarios while the Zroute technology within IC Compiler was used to generate DRC clean wires. Samsung Foundry used the PrimeTime® SI timing analysis solution together with accurate extraction from StarRC™ to analyze implications of on-chip variation and reduced wire spacing.

"The Galaxy Platform consistently demonstrates the ability to handle the most challenging designs," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Synopsys leads the effort to enable semiconductor manufacturers to achieve success in production designs at each successive technology node, as shown by the results of our close interaction with Samsung Foundry. Our large investment in R&D and collaborative approach are enabling our customers to achieve first-pass silicon success in such advanced nodes as 32-nanometers. We look forward to continue our collaboration with Samsung Foundry to develop next-generation flows."

Galaxy Implementation Platform

The Galaxy Implementation Platform is a comprehensive solution for cell-based and custom IC implementation. Galaxy accepts design intent in industry standard formats and generates a production-ready IC design in GDSII format. Galaxy RTL and physical implementation concurrently balance design constraints by performing intelligent tradeoffs between speed, area, power, test and manufacturability. Galaxy signoff engines accurately model complex physical interactions to ensure signal and power integrity. Coherent algorithms for parasitic extraction and timing produce correlated results.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, systems-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

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